1.1 General Description

The TSX DMR 1652 fast I/O coprocessor is an intelligent module that has 8 fast inputs and 8 fast outputs (24 VDC). It is designed for applications that require short response times (1 to 10 ms) and/or guaranteed response times (± 0.50 ms), and in particular for applications requiring:

- The acquisition of transient or rapid events, with or without memorization, that may require an immediate action on the process,
- The control of actions, independently of the user program or CPU, with short (1 ms), guaranteed time delays,
- The monitoring of the application cycle times, including that of the Fast task, or of the duration of an event (watchdog timer function),
- The rapid counting of parts or events (at a rate of up to 1 KHz) with threshold monitoring.

1.1-1 Module Operation and Logic Functions

The four user-selectable logic functions that can be configured and assigned to the inputs and outputs of the module are as follows:

Like all intelligent modules of the TSX Series 7 range, the TSX DMR 1652 operates on the complete I/O bus and communicates with the CPU through its Discrete interface and its Register interface (the Message interface is not used).

The module permanently reads its 8 fast inputs, which have reduced filtering. When a change of state occurs, the module can generate interrupt signals (through its Discrete interface) according to the conditions (validation, rising or falling edge) dictated by the user program in the memory of the CPU. These interrupt signals have the effect of jumping the program scan to the Interrupt task, which has the highest priority.

The module's 8 transistor outputs can be controlled by the module itself through integrated logic functions that can be selected and configured by the user.

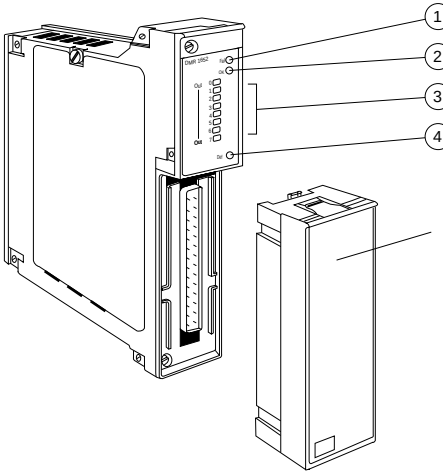
These 2 types of operation (generation of interrupts, outputs controlled by the module) are compatible and can be used simultaneously.

Function 0: Boolean logic,
Function 1: Bistable latch (RS flip-flop),
Function 2: Timer/Monostable,
Function 3: Counting with threshold monitoring.

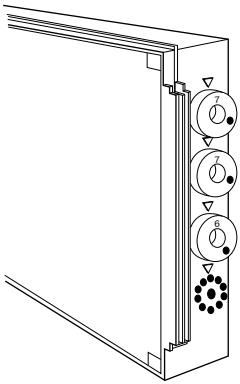
1.2 Physical Description

The TSX DMR 1652 fast I/O coprocessor is the same size as the other I/O module and can be installed in any slot of the TSX 47-30 and TSX 67/87 racks equipped with the complete I/O bus, or the first 4 slots of the TSX 47-20 (see Section 4 for installation details).
The front panel of the model is equipped with a set of indicator lights and a connector for receiving terminal block BLK4.
The rear panel of the module is equipped with three factory-coded locating devices (code 776).

① Fail : This LED is off during normal operation,
② OK : This LED is on during normal operation, it goes off if the terminal block is opened or a module fault occurs,
③ Out i: This LED shows the output state,
④ Def : This LED is off in normal operation, on if a short circuit occurs on one of the outputs.

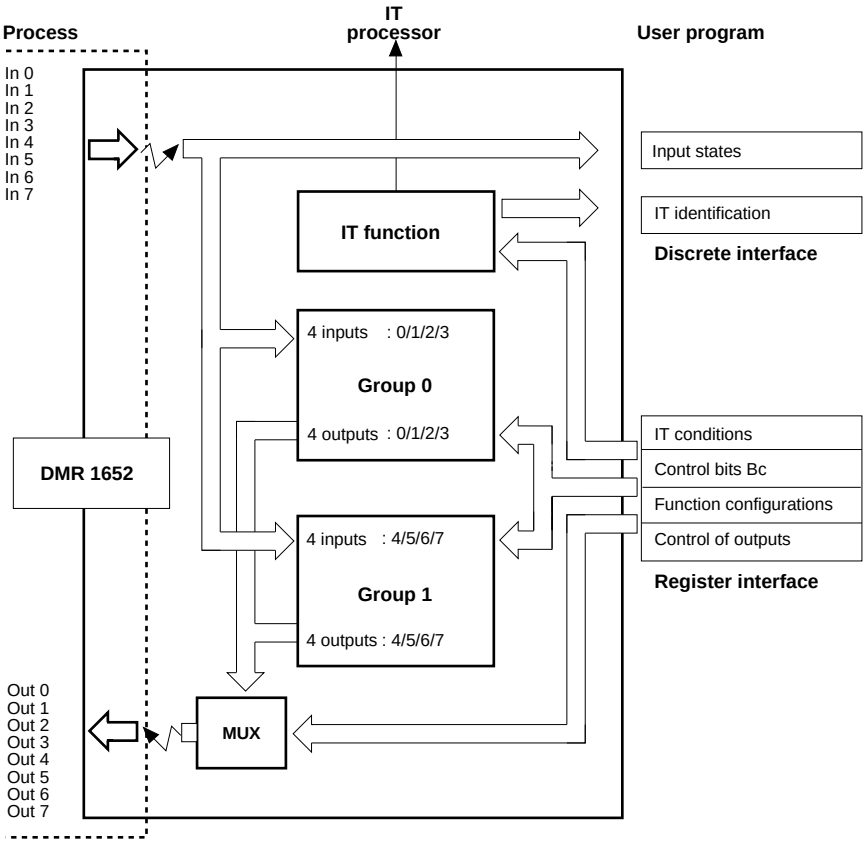


Factory-coded locating devices: code 776



Software code: See Sub-section 4.1

2.1 Structure



2.1-1 Exchanges with the PLC Processor

In the TSX 47-20 only:

- The interrupt (IT) function is not available as this PLC has no Interrupt task,
- The time required by the TSX 47-20 to exchange one register word with an intelligent module is **twice** the scan time of the PLC.
  This factor must be taken into account in applications where the outputs of the TSX DMR 1652 module are controlled by user program.

In the TSX 47-30 and TSX 67/87 PLCs, all the functions of the module are available without restriction.

2.2 Dialog with the PLC

2.2-1 Discrete Interface

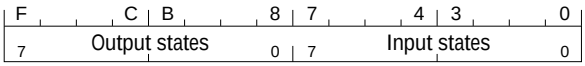
The TSX DMR 1652 fast I/O coprocessor module has:
- 8 isolated inputs (In0 to In7) which can generate 8 interrupts according to the conditions (validation, rising or falling edge) dictated by the user program,
- 8 isolated and protected transistor outputs (Out0 to Out7) which can be controlled by either:
  - the user program,
  - the module itself through predefined logic functions.

The communication between the module and the PLC is established through the Discrete interface and the Register interface of the module.

Note: The Message interface is not used in the TSX DMR 1652 module.

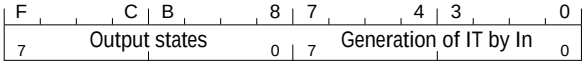
The Discrete interface is used to transfer information concerning the I/O states and the generation of interrupts.

In the TSX 47-20



Ixy,i

In the TSX 47-30 and TSX 67/87



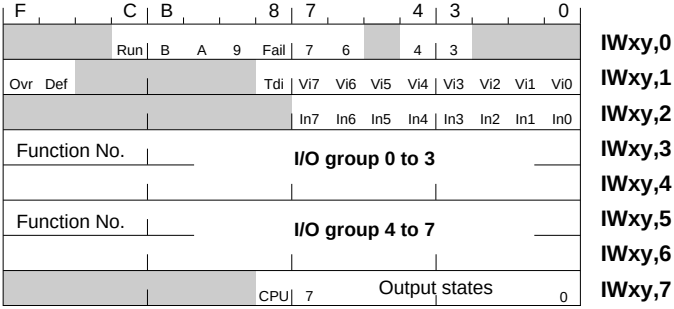
Ixy,i

When the module is stopped, the output states are at 0.

2.2-2 Register Interface

The input word registers (IW) and output word registers (OW) are grouped according to the way they are used, as follows:
- Standard registers (IW/OWxy,0), used in the same way as in the other intelligent modules,
- Interrupt control registers (IW/OWxy,1 and 2), whose values can change during the operation of the module,
- Logic function configuration registers (IW/OWxy,3, 4, 5 and 6). Certain bits can change state during operation. The logic functions can be configured only when the module is stopped,
- Output control registers (IW/OWxy,7).

Data stored in the input register words:

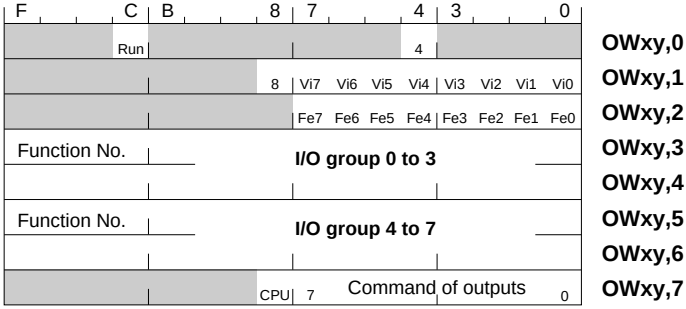


Bit not used

Register word	Bit	Function
IWxy,0,	**C** : 1	= module running,
IWxy,0,	**B** : 1	= module not configured,
IWxy,0,	**A** : 1	= terminal block open or absent,
IWxy,0,	**9** : 1	= initial self-test in progress,
IWxy,0,	**8** : 1	= module failure (Fail),
IWxy,0,	**7** : 1	= application fault (Ovr or Def),
IWxy,0,	**6** : 1	= blocking fault,
IWxy,0,	**4** : 1	= presence of a fault (except Fail),
IWxy,0,	**3** : 1	= module available (self-test finished),
IWxy,1,	**F** : 1	= overrun fault (Ovr),
IWxy,1,	**E** : 1	= short-circuit on one of the outputs (Def),
IWxy,2,	**0 to 7** :	input states updated with a period of 1 to 10 ms (In0 to 7).

The other bits reflect the states of the control bits (recopy of the bit states of the output register words).

Data stored in the output register words:



Bit not used

Register word Bit Function

OWxy,0, C : 1 = activates the configured logic function (module set to Run),

OWxy,0, 4 : 0 = interrupt system not validated,

1 = validation of the events generating interrupts,

OWxy,1, 8 : 1 = cancellation of the 100 ms time delay of interrupts (Tdi), (see Section 3.5)

OWxy,1,0 to 7 : 0 = the corresponding input cannot generate an IT (Vi0 to 7),

OWxy,2,0 to 7 : 1 = IT on a falling edge of the corresponding input (Fe0 to 7),

0 = IT on a rising edge of the corresponding input,

OWxy,7, 8 : 1 = control by the user program of the 8 outputs. The states of the 8 outputs are contained in the least significant byte (OWxy,7,0 to OWxy,7,7).

2.2-3 Interrupts

This function is available only with the TSX 47-30 and TSX 67/87. It is not available with the TSX 47-20 as this PLC has no Interrupt task.

The TSX DMR 1652 module has eight 24 VDC inputs, each of which can deliver an interrupt (IT) signal to the CPU.

The user program defines the interrupt conditions for each input: IT validated or not (Vi0 to 7) and IT on a rising or falling edge (Fe0 to 7).

2.3 Operating Modes of the Module

2.3-1 Description

The TSX DMR 1652 fast I/O coprocessor module has 3 operating modes as follows:
- Self-test (this is a transient state that occurs on power-up or when the module is plugged into a powered up PLC),
- Stop mode,
- Run mode.

2.3-2 Action on the Operating Modes

Self-test
The self-tests are executed each time the module is powered up; they monitor and process the internal faults of the module.
During the self-tests, the outputs of the module are set to 0.
If no faults have been detected at the end of the self-tests, the OK light comes on and the "module available" bit is set to 1.

Stop mode
In the Stop mode the module is inactive, whether it has been configured or not, and the states of the inputs and outputs in the image memory are at 0.
A Stop command from the CPU causes the re-initialization of the module and the acquisition of the configuration contained in the output register words OW.

Run mode
In the Run mode the module is fully operational. Any changes in the parameters of the selected logic function are taken into account, but the type of logic function (F0 to F3) cannot be changed (it can only be changed in the Stop mode).
A Run command from the CPU causes the validation of the configuration. If the configuration is not correct, the "not configured" bit is set to 1.
The Run command and the configuration can be sent simultaneously after the self-tests.

2.3-3 Effect of Stopping the PLC

Stopping the PLC has no effect on the 8 inputs of the module and effects the 8 outputs of the module only in the following case:
- if SY8 = 1 (value by default) the outputs are reset to 0,
- if SY8 = 0, the outputs are activated normally.

Note: If the configuration of the PLC includes local or remote extension racks, the states of system bits SY32 to SY39 must be taken into account as well as the state of system bit SY8 (refer to the TSX T607 Programming Terminal User's Manual, Book 1, Section 10.3).

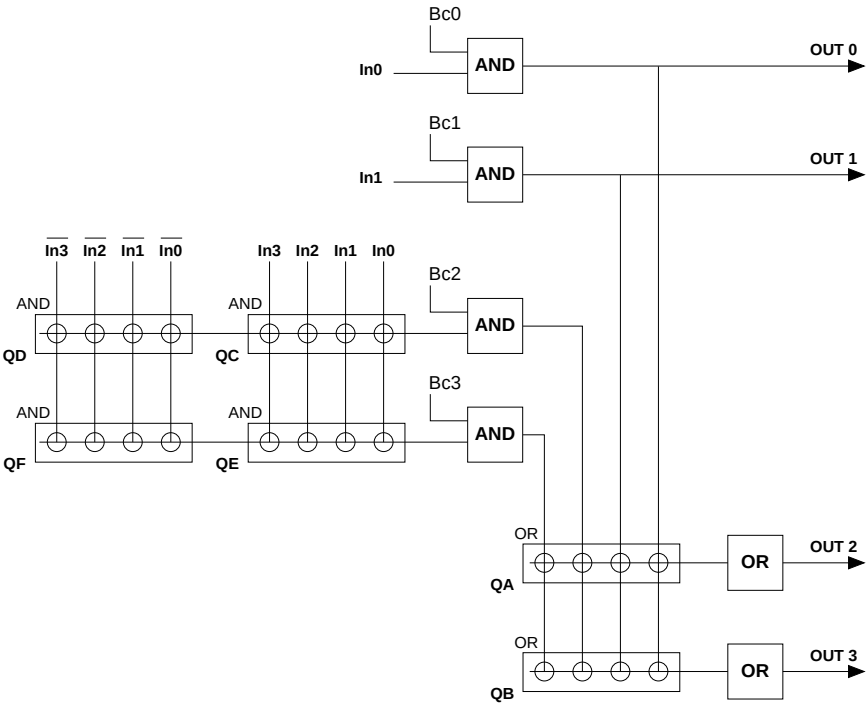
3.1 Function 0: Boolean Logic

3.1-1 Description of the Function

This logic function is intended for applications that require an immediate reaction to an external event when the validation conditions are true.
Typical examples of use include:

- The step by step advance of a sequential machine,
- The automatic selection or rejection of parts,
- The marking or stamping of parts.

Group 0:



The logic functions are the same for Group 1 (In4 to 7 and Out 4 to 7).

The functions are parameterized by defining the 6 nibbles (4-bit bytes) QA, QB, QC, QD, QE and QF, which correspond to the logic connections of the functions.

The bits Bc0 to 3 are the validation condition bits that are supplied by the user program through the output word register interface OW. The acquisition of these bits by the module is indicated to the CPU through the input word register interface IW.

3.1-2 Parameterizing the Functions

The functions are parameterized through the register interface by OWxy,3 and 4 for Group 0 and by OWxy,5 and 6 for Group 1.

Group 0

F … C	B … 8	7 … 4	3 … 0	
0	Bc3 Bc2 Bc1 Bc0	**QB**	**QA**	**OWxy,3**
QF	**QE**	**QD**	**QC**	**OWxy,4**

Group 1

F … C	B … 8	7 … 4	3 … 0	
0	Bc7 Bc6 Bc5 Bc4	**QB**	**QA**	**OWxy,5**
QF	**QE**	**QD**	**QC**	**OWxy,6**

3.1-3 Example

Assignment of the following logic functions to Out0 to 2:

Out 0 = Bc 0. In 0

Out 1 = Bc 1. In 1

Out 2 = (Bc 2. $\overline{\text{In 3}}$) + (Bc 3 • In 2 • $\overline{\text{In 0}}$)

OWxy,3,	0/3	**QA** =	1 1 0 0	→ **H 'C'**
OWxy,3,	4/7	**QB** =	0 0 0 0 (see **Note**)	→ **H '0'**
OWxy,3,	8/B	**Control** =	1 1 1 1	→ **H 'F'**
OWxy,3,	C/F	**Function No.** =	0	→ **H '0'**

H '0 F 0 C' -> OWxy,3

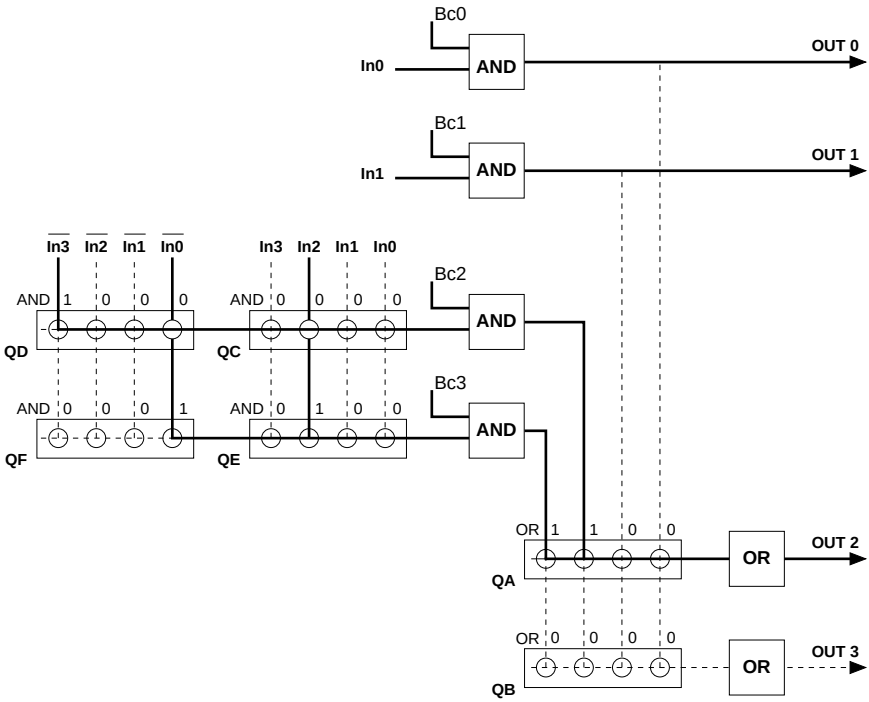
OWxy,4,	0/3	**QC** =	0 0 0 0	→ **H '0'**
OWxy,4,	4/7	**QD** =	1 0 0 0	→ **H '8'**
OWxy,4,	8/B	**QE** =	0 1 0 0	→ **H '4'**
OWxy,4,	C/F	**QF** =	0 0 0 1	→ **H '1'**

H '1 4 8 0' -> OWxy,4

Note: The four validation condition bits Bc0 to 3 do not have to be written when the functions are parameterized; their states can be defined at any time by the user program by writing output word OWxy,3.

Writing the register words OWxy,3 and OWxy,4 (with the module in the Stop mode) implements the logic diagram below. A run command by the bit OWxy,0,C is then necessary to execute the logic function.

Group 0:



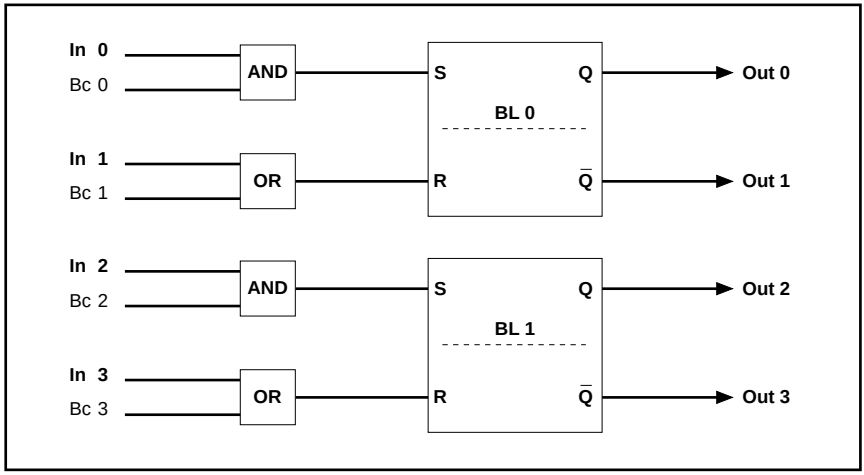
3.2 Function 1: Bistable Latch

3.2-1 Description of the Function

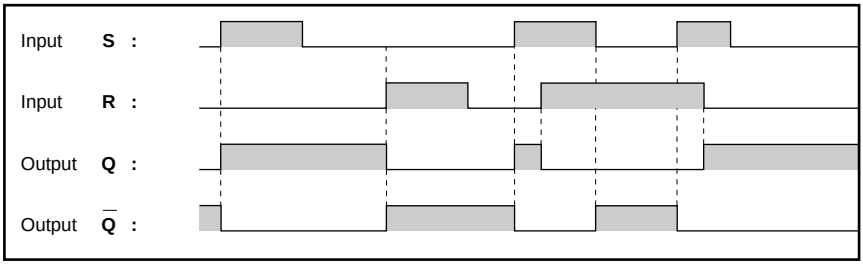
This logic function is intended for applications that require the memorization of a transient external event, or the activation of an output during a period determined by two external events, for example:

- The memorization of a transient contact with acknowledgement by the program or externally,
- The application of a strip of glue slaved to the change of state of 2 position detectors.

Group 0



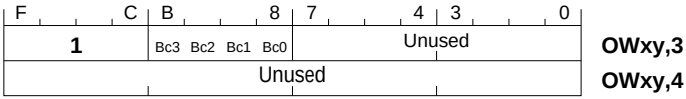
The logic functions are the same for Group 1 (In4 to 7).



3.2-2 Parameterizing the Functions

The functions are parameterized through the register interface by OWxy,3 and 4 for Group 0 and by OWxy,5 and 6 for Group 1.

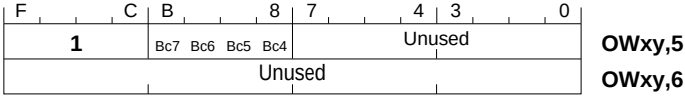
Group 0



OWxy,3

OWxy,4

Group 1



OWxy,5

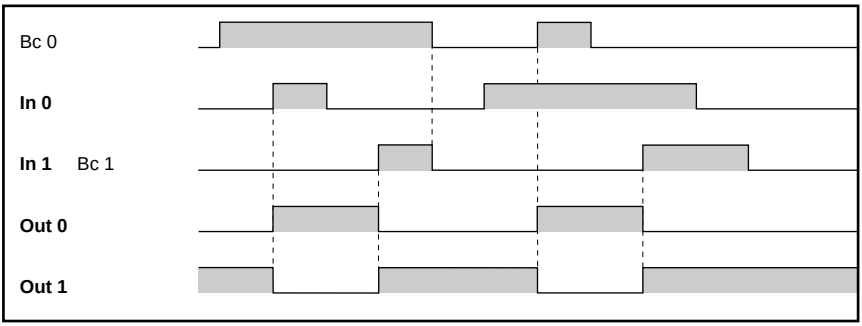
OWxy,6

3.2-3 Example

Implementation of the bistable latch function with inputs In0 and In1.

H'1100' → **OWxy,3** with H'1100'

Bc 0 = 1
Bc 1 = 0
Bc 2 = 0
Bc 3 = 0

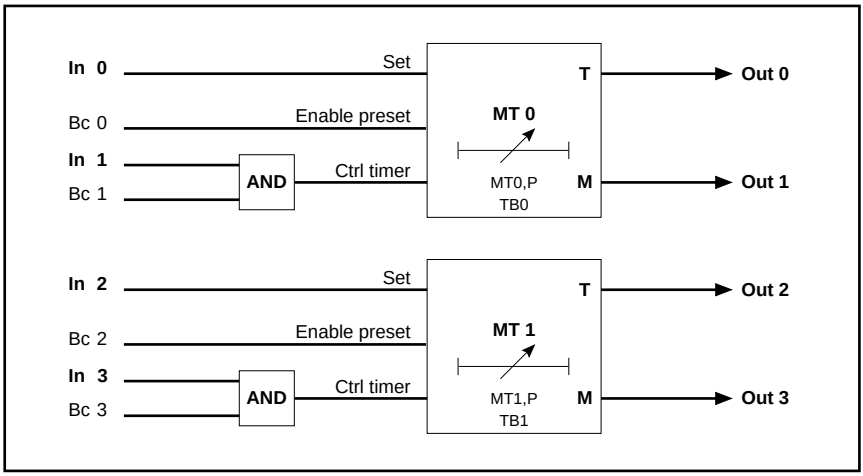


3.3 Function 2: Timer/Monostable

3.3-1 Description of the Function

This logic function is intended for applications that require short, guaranteed response times (timer and monostable), for example:
- The application of a strip of glue slaved to a time factor,
- The watchdog monitoring of the tasks (execution of the program).

Group 0



The logic function are the same for Group 1 (In4 to 7 and Out4 to 7).

Commands:

- Preset : MT0,P/MT1,P — On a rising edge of Set with Enable preset at 1 (preset value → current value),
- Run : If the current value ≠ 0 and Ctrl timer is at 1,
- Freeze current value: Ctrl timer = 0.

Outputs

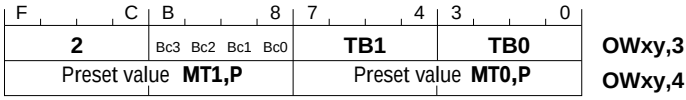
- **T** (done) **= 1** : if current value = 0 and Set and Ctrl timer are at 1,
- **M** (running) **= 1** : if current value ≠ 0 and Set and Ctrl timer are at 1,
- **T = 0** and **M = 0** : if Ctrl timer is at 0.

Remarks: The preset value **MTi,P** and the time base **TB** can be modified with the module running. The new values are not loaded into the IW register until the preset command is given.
During the initialization sequence, if the Set and Enable preset inputs are at 1, the preset value is not loaded (since there must be a rising edge on the Set input to load the preset value).

3.3-2 Parameterizing the Functions

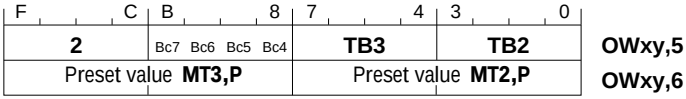
The functions are parameterized through the register interface by OWxy,3 and 4 for Group 0 and by OWxy,5 and 6 for Group 1.

Group 0



OWxy,3
OWxy,4

Group 1



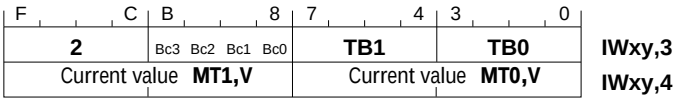
OWxy,5
OWxy,6

The time base values are configured as follows:
- **0** for 1 ms
- **1** for 10 ms
- **2** for 100 ms

The preset values vary from 0 to 255 and are entered in hexadecimal code.

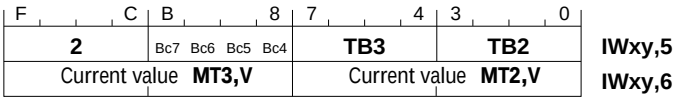
The parameters are accessible by the user program in the IW register (in hexadecimal code for the current values MTi,V).

Group 0



IWxy,3
IWxy,4

Group 1



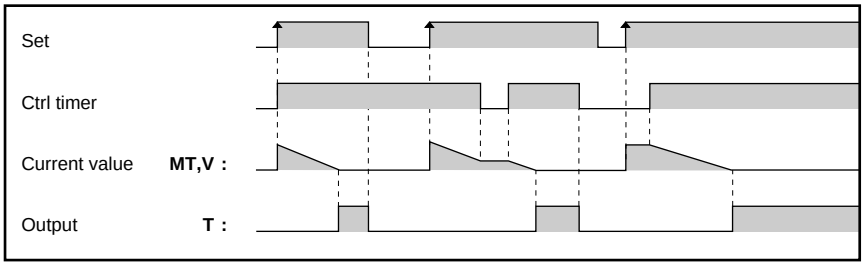
IWxy,5
IWxy,6

3.3-3 Typical Timing Diagrams

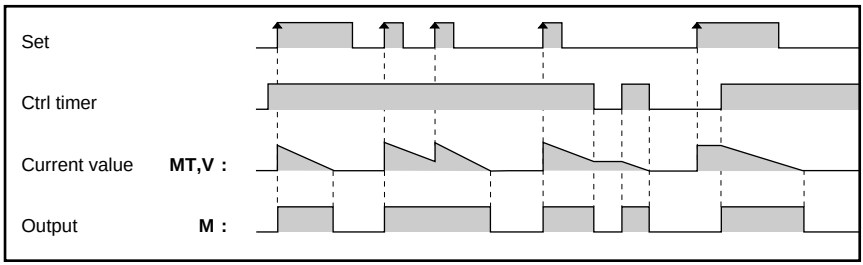
The timing diagrams below are given as examples of the use of the timer and monostable functions.

It is assumed that the Enable preset input is always at state 1.

Timer function



Monostable function



3.3-4 Example

Configure function MT0 with a time base TB of 1 ms and a preset value of 155 ms.

H'2300'→ OWxy,3 with H'2300'
H'9B' → OWxy,4 with H'9B'

FB = 1 ms
Bc0 = 1 (Enable Preset 1)
Bc1 = 1 (Ctrl timer 0)
Bc2 = 0 (Enable Preset 1)
Bc3 = 0 (Enable Preset 1)

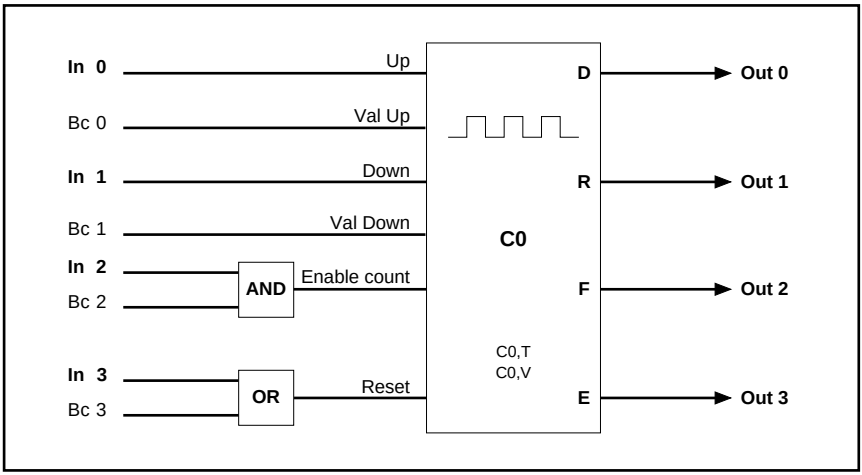
MT0,P = 155 (Decimal value)

3.4 Function 3: Counter

3.4-1 Description of the Function

This function is intended for applications that require the counting of parts or events, for example filling/packing, palletization, stock control, etc.

Groupe 0:



The logic functions are the same for Group 1 (In4 to 7 and Out 4 to 7).

Commands

- Count up : on a rising edge of the Up input if the Val Up input = 1 and the Reset input = 0,
- Count down: on a rising edge of the Down input if the Val Down input = 1 and the Reset input = 0,
- Freeze : Enable count = 0 and Reset = 0,
- Reset to 0 : Reset = 1 (this input has the highest priority).

Outputs

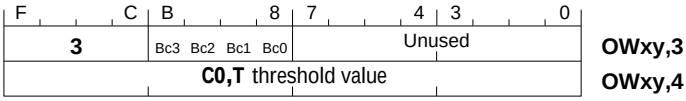
- **F** Full : upcounting overflow output (the current value Ci,V changes from +32767 to -32768),
- **D** Done : current value Ci,V ≥ threshold value Ci,T,
- **R** Run : current value Ci,V < threshold value Ci,T,
- **E** Empty : downcounting overflow output (the current value Ci,V changes from -32768 to +32767).

Remarks: The freezing of the current value by Enable count has no action on the outputs. The overflow indicators F and E are memorized and acknowledged when the Reset input = 1. The counter has no preset value.
During the initialization sequence, the current value Ci,V is at 0.
The outputs D and R are set according to the threshold value Ci,T.

3.4-2 Parameterizing the Functions

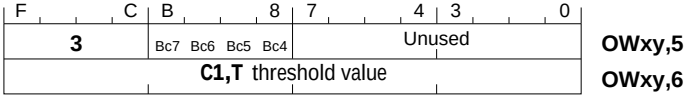
The functions are parameterized through the register interface by OWxy,3 and 4 for Group 0 and by OWxy,5 and 6 for Group 1.

Group 0



OWxy,3
OWxy,4

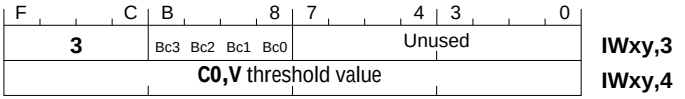
Group 1



OWxy,5
OWxy,6

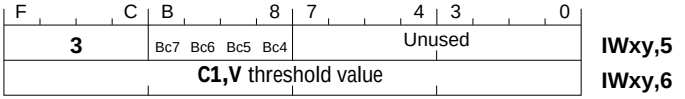
The parameters are accessible by the user program in the IW register (in hexadecimal code for the current values Ci,V).

Group 0



IWxy,3
IWxy,4

Group 1



IWxy,5
IWxy,6

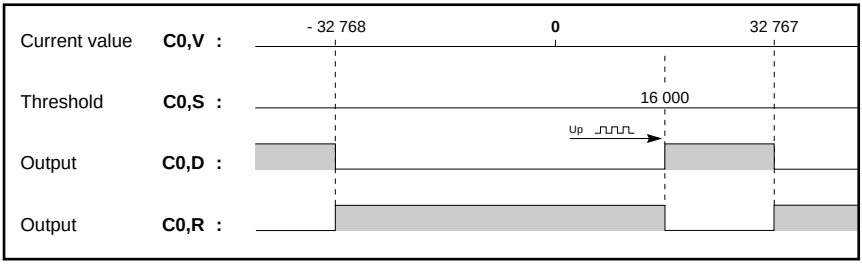
3.4-3 Example

Counter C0 with a threshold value C0,T of 16 000.

H'3500' → **OWxy,3** with H'3500'
16 000 → **OWxy,4**

- Bc0 = 1 (Val Up)
- Bc1 = 0 (Val Down)
- Bc2 = 1 (Enable Count)
- Bc3 = 0 (Reset)

Timing diagram:



3.5 Interrupt Inputs

3.5-1 Description and Configuration of the Function

This function is available with the TSX 47-30 and TSX 67/87 only.

The user program validates whichever of the 8 inputs are to generate an interrupt to the CPU (Vi = 1 in register word OWxy,1 (bits 0 to 7)).

It also defines for each input validated for IT the event causing the IT:

- Rising edge (Fe = 0),
- Falling edge (Fe = 1)

in register word OWxy,2 (bits 0 to 7)

The edge thus defined causes:

- The interruption of the CPU, if it can be interrupted (OWxy,0,4 = 1).
- The setting to 1 of the bit corresponding to this input in the Discrete interface (Ixy,0 to 7).

The same input cannot normally interrupt the CPU twice in less than 100 ms. However, this time delay can be cancelled for all the inputs by the user program (OWxy,1,8 = 1).

The parameters of the logic function can be changed with the module running.

3.5-2 Operation

Each input can, by configuration, generate an interrupt that has the effect of jumping the program scan to the Interrupt task (programmed by the user), thus permitting a rapid, programmed response to an external event.

After the CPU has been interrupted by one input, the interrupt requests from other inputs are memorized and processed as soon as the Interrupt task becomes available (end of processing and acknowledgement of IT in progress).

The time required to transfer an interrupt to the CPU is 1 ms.

Remarks: If the normal 100 ms time delay of the interrupts is cancelled (by setting OWxy,1,8 to 1), the user must take the necessary precautions to deal with interruptions of the CPU that may be too frequent.
It is possible to eliminate the processing time of the module and to reduce the transfer time of the interrupts to 200 µs by configuring the group concerned for Function 0 with all the parameters at 0:

H'0' → OWxy,3 → OWxy,4 for Group 0 (In0 to 3),
H'0' → OWxy,5 → OWxy,6 for Group 1 (In4 to 7).

3.5-3 Example

Description of the function:

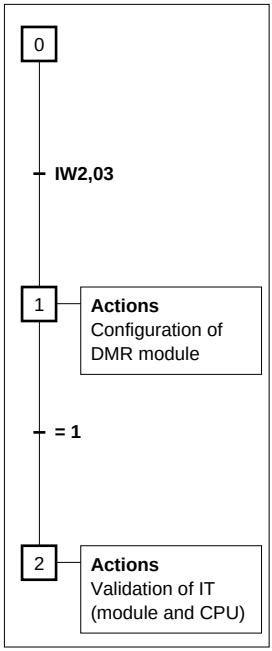
The TSX DMR 1652 is installed in slot 2 of rack 0. The interrupt inputs are In0 and In1.

- On a rising edge of In0 the PLC output O17,0 is set to 0,
- On a falling edge of In1 the PLC output O17,0 is set to 1.

Note: This example is given for information only. In reality, the TSX DMR 1652 is capable of performing the function described above independently of the CPU by using the bistable latch function F1.

Programming of the Master task:

The Grafcet representation below is used to show the various preparatory phases in graphic form. In a real application, the Grafcet steps are implemented by internal bits programmed in Ladder or Literal language (the Grafcet being reserved for the sequential processing of the application).



Initialization

Module available

Module set to Run
Selection of IT on In0 and 1
Selection of type of edge causing IT
Resetting to 0 of the rest of the configuration

```
H'1000' → OW2,0 ;
H'0003' → OW2,1 ;
H'0002' → OW2,2 ;

0 → OW2,2 → OW2,3
  → OW2,4 → OW2,5
  → OW2,6 → OW2,7
```

Validation of module IT
Demasking of CPU IT
Activation of IT task

```
SET OW2,0,4 ;
DMASKINT (I2) ;
START CTRL1
```

Programming of the Interrupt task

```
< IT generated by DMR ?
! READINT (I2;B2)

< If IT   from DMR, read DMR discrete bits
! IF B2   THEN READBIT (I2;B10)
          ELSE JUMP L10

< If IT from DMR, transfer the image of the output bits of
  module 17 to the Bi zone for updating
! O17,0 [8] → B20 [8]

< Updating according to the origin of the IT (In0 or In1)
! IF B10 THEN RESET B20
! IF B11 THEN SET  B20

< Explicit exchange of output module 17, confirmation of the
  image of the output bits, and acknowledgement of the IT
! WRITEBIT (B20;I17); B20 [8] → O17,0 [8];
  ACKINT (I2)

< Processing corresponding to the IT from another module or
  end of IT task

! L10
```

4.1 Installation

4.1-1 Possible Locations

As a general rule, the TSX DMR 1652 module can be installed in any rack that is equipped with the complete bus.

Basic configuration	TSX 47 20 ..	Slots 0 to 3. Interrupt inputs not available.
Basic configuration (single rack)	TSX 47 300 TSX 67 200	Any slot, 5 intelligent modules max. Interrupt inputs available.
Basic configuration (double rack)	TSX 67 300 TSX 87 120 TSX 87 200 TSX 87 300	Slots 0 to 7 of the lower rack. Interrupt inputs available.
Local extension racks (single)	TSX RCE 860	Any slot. Interrupt inputs available (*)
Remote extension racks (single)	TSX RCF 860	Any slot. Interrupt inputs available (**)
Local extension racks (double)	TSX RDE 880	Slots 0 to 7 of the lower rack. Interrupt inputs available (*)

Restrictions: (*) The TSX 67-300 and TSX 87-120/200 cannot process interrupts from extension racks (see page 40).
(**) The TSX 67-300 and TSX 87-120/200 cannot accept intelligent modules in remote extension racks.

Warning
The TSX DMR 1652 module should never be installed in the upper half of a double rack (wiring impossible and risk of damage).

4.1-2 Configuration

The TSX DMR 1652 has two types of configuration codes:

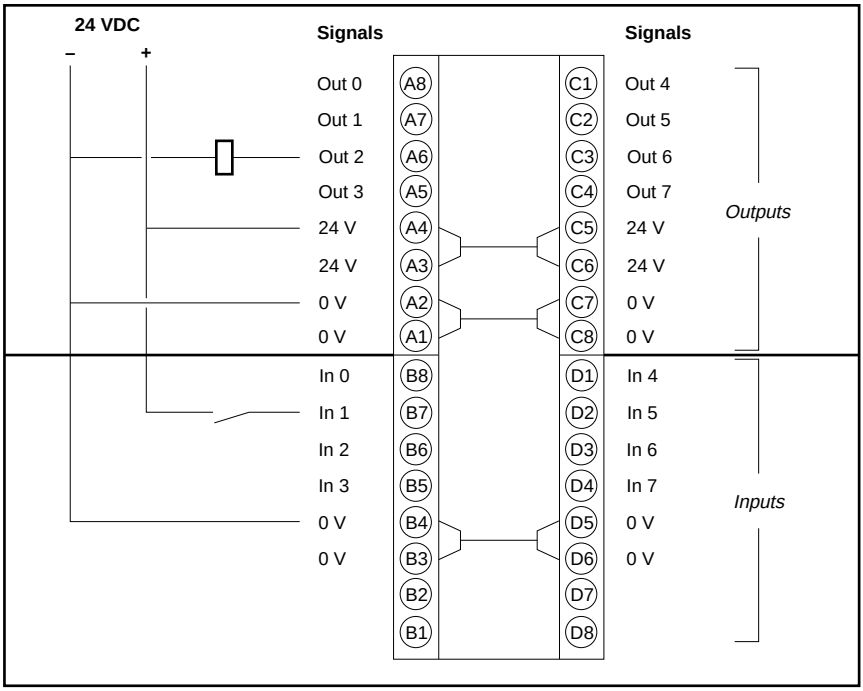
- A **hardware configuration code**, which is coded ex-factory on the 3 female locating devices on the back of the module,
- A **software configuration code**, which is entered on the TSX T607 or TSX T407 terminal during the configuration of the inputs and outputs.

Codes	TSX 47-20	TSX 47-30 TSX 67/87
Hardware	77	776
Software	62	776 or 62

4.2 Wiring

4.2-1 Wiring the Terminal Block

Terminal block to be used: TSX BLK 4.



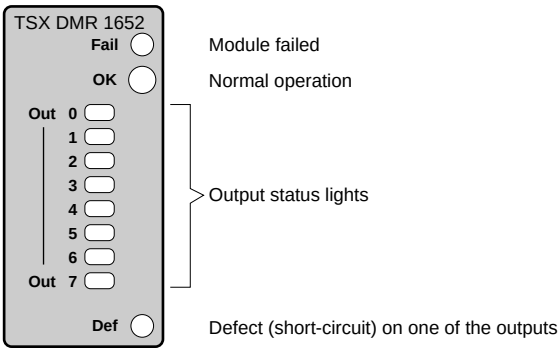
The connections between the 0 V terminals or 24 V terminals are made by the module. The module does not supply the 24 VDC power.

4.2-2 Wiring Precautions

The wiring precautions are the same as for the discrete I/O modules of the TSX Series 7 range. Refer to the installation manual of the PLC concerned.

5.1 Indicator Lights

Front panel indicator lights:



5.2 Troubleshooting

5.2-1 Types of Faults

- **Open terminal block:** Unlocking the terminal block resets all the outputs of the module to 0. The **OK** light goes out and bit B of the I/O status word is set to 1, this word can be accessed by the TSX T407 terminal in the Diagnostic mode.

- **Short-circuit on one output:** When an output of the module at state 1 is short-circuited for more than 100 ms, the output is forced to 0 and the **Def** light comes on until the fault is acknowledged by opening the terminal block or cutting off the power supply to the outputs of the module.

- **Overrun:** When the total frequency of the input signals is too high (see Section 6.2), the IW and OW register exchanges are blocked (the user program loses control of the module) and the module is forced to the Stop mode after 10 ms.

- **Module fault:** If a fault is detected during the self-tests, the module is blocked. The **Fail** light comes on and the **OK** light goes out.

5.2-2 Diagnostics

DMR light	PLC I/O light	Fault bits at 1	Type of fault	Consequences on the module	Acknowledgement of the fault
Fail on OK out	On	IWxy,0,8	Internal fault detected by self-tests	µP reset	Module de-energized (1)
OK out Fail out	On	IWxy,0,6 IWxy,0,4	Fault of IT controller detected by self-tests	Blocking fault	Module de-energized (1)
OK out Fail out	On	IWxy,0,A IWxy,0,6 IWxy,0,4	Terminal block open or faulty	Forced to Stop (2)	Close terminal block and command Stop of module
OK on	Out	IWxy,1,F IWxy,0,7 IWxy,0,4	Overrun (1) or application fault (3)	Forced to Stop (2)	Command Stop then Run of module
Def on OK on	Out	IWxy,1,E IWxy,0,7 IWxy,0,4	Short-circuit on one output, or application fault	Output forced to 0	Open the terminal block or de-energize the actuator (4)

Remarks:

(1) If the fault persists, change the module.

(2) When the module is stopped, its outputs are reset to 0.

(3) An overrun fault is detected when the total number of changes of state of the inputs is more than 2400 and less than 10,000 (above 10,000 no detection is possible).

(4) The fault concerning a short-circuit on one of the outputs (Def) does not disappear until the terminal block is opened or the power supply to the outputs of the module is cut off.

See Section 2.3: Operating Modes of the Module.

Note: The faults that cause the I/O fault lights to come on (on the front of the processor or extension module of the PLC) also cause:

- SY10 = 0,
- SY40 to 47 = 0, depending on the rack concerned,
- Oxy,S = 1 for the faulty module.

6.1 Technical Characteristics

6.1-1 Characteristics of the Module

Inputs	8 fast inputs for 24 VDC signals, commoned to the 0 V of the power supply.
Outputs	8 transistor outputs, 24 VDC/350 mA positive logic, protected against short circuits and overvoltages. Common supply to the 8 outputs (loads commoned to 0 V).
Compatibility	Inputs: Compatible with CELENEC 2 or 3 wire detectors. Compatible with 24 VDC transistor outputs (PNP). Compatible with 24 VDC output modules of the TSX Series 7 range. CONFORMING TO IEC 2 AND NFC 63850 STANDARDS
	Outputs: Compatible with solenoids of < 8W, Compatible with lamps of < 5W, Compatible with all input modules of the TSX Series 7 range. The outputs can be reconnected to the inputs.
Functional capacities	• Counting : 16 bits (-32768 to +32767), • Timing : 8 bits (0 -1023 increments), time bases: 1 ms, 10 ms, 100 ms.
Temperature limits	• Operation : 0 to +60°C, • Storage : -40 to 70°C.

6.1-2 Characteristics of the Inputs

Nominal input values			
• Voltage	24 VDC		
• Current	15 mA		
• Sensor power supply	19.2 to 30 VDC		
Limit input values			
• at state 1 voltage	11 to 30 VDC		
current	6 to 19 mA		
• at state 0 voltage	V ≤ 5 VDC		
current	I ≤ 3 mA		
Input impedance	1500 to 1700 ohms		
Response times:			
• from state 0 to 1	Min 0.1 ms	Typ 0.2 ms	Max 0.5 ms
• from state 1 to 0	Min 0.1 ms	Typ 0.2 ms	Max 0.5 ms
Power dissipation	360 mW (at nominal voltage)		
External line:			
• permissible line resistance	R ≤ 500 ohms		
• permissible leakage resistance	R ≥ 30 Kohms		
Isolation			
• between input circuits and internal bus	1500 V (rms)		50/60Hz
• between input circuits and electrical or mechanical ground	R > 10 Mohms at 500 VDC		

6.1-3 Characteristics of the Outputs

Nominal values	
• nominal voltage	24 VDC
• nominal current	≤ 0.35 A
• current limitation	by thermal circuit-breaker
Limit values	
• voltage	19.2 to 30 VDC
• current	0.44 A for one output
• current for all 8 outputs	≤ 2.8 A with ventilated rack
Response times	
• from state 0 to 1	< 100 µs
• from state 1 to 0	< 500 µs
Leakage current at state 0	< 0.1 mA
Residual voltage at state 1	< 1.3 V
Protection	
• against overloads	thermal circuit-breaker
• against inductive overvoltages	discharge and clipping diodes
Power dissipation	0.6 W (nominal voltage)
Power consumption	60 mA
Isolation	> 10 Mohms at 500 VDC

Note: In case of power loss due to a short-circuit or overload, it is necessary to de-energize the actuators or remove and replace the terminal block to rearm the module.

6.1-4 Power Consumption

PLC output voltage	+5V	+24V
TSX DMR 1652 consumption	350 mA	15 mA

If the module is installed in a rack that is not ventilated, UL standards impose the following limitations:

- **Inputs** The number of inputs continuously at state 1 must not exceed 5,
- **Outputs** The total current for all 8 outputs must not exceed 1.7 A.

6.2 Performance Characteristics

6.2-1 Function 0: Boolean Logic

To obtain the performance characteristics described below, the following conditions must be respected:

- Minimum duration of an input state: 1 ms,
- Maximum rate of change of all 8 inputs: 10 changes of state in 10 ms, with 2 changes of state maximum per millisecond.

Performance:

- Input/Output transfer time: 1 ms max.

6.2-2 Function 1: Bistable Latch

To obtain the performance characteristics described below, the following conditions must be respected:

- Minimum duration of an input state: 1 ms,

Performance:

- Input/Output transfer time: 1 ms max.

6.2-3 Function 2: Timer/Monostable

To obtain the performance characteristics described below, the following conditions must be respected:

- Minimum duration of an input state: 1 ms,

Performance:

- Input/Output transfer time: 1 ms max.,
- Time base resolution: 1 ms,
- Time base jitter: ± 0.5 ms.

6.2-4 Function 3: Counter

To obtain the performance characteristics described below, the following conditions must be respected:

- Minimum duration of an input state: 1 ms,

Performance:

- Input/Output transfer time: 1 ms max.,
- Maximum count rate: 500 Hz.

Note:

It is possible to increase the maximum count rate by limiting the performance of the function that is implemented on the other group, for example:

- Counter implemented on Group 0,
- Functions authorized on Group 1: F0, F1 or F2,
- Minimum duration of a state on the counter input: 500 µs,
- Minimum duration of a state on the inputs of Group 1: 5 ms,
- Maximum rate of change of Group 1 inputs: 2 changes of state in 10 ms, with 2 changes of state maximum per millisecond.

In these conditions, the performance of the counter is as follows:

- Input/Output transfer time: 1 ms max.,
- Maximum count rate: 1 KHz.

6.2-5 Interrupt Function

The time required to activate the Interrupt task in the TSX 47-30 and TSX 67/87 the sum of two times (**tic + tip**).

- **tic:** time between the change of state of the interrupt input and the presence of the IT signal on the I/O bus.
  tic = 1 ms for the TSX DMR 1652 module.
- **tip:** time between the presence of the IT signal on the I/O bus and the activation of the Interrupt task. This time depends on the type of PLC and whether local or remote extension racks are used, as shown in the table below.

Maximum time **tip**	Local I/O (TSX LES)		Remote I/O (TSX LFS)	
	Basic config.	Extensions (1)	Basic config.	Extensions (2)
TSX 47-30	1.5 ms	-	-	-
TSX 67-20	1.5 ms	1.5 ms	2.2 ms	2.2 ms
TSX 67-30	2.5 ms	-	3.2 ms	-
TSX 87-10/20	2.5 ms	-	3.2 ms	-
TSX 87-30	1 ms	1 ms	1.7 ms	1.7 ms

(1) Reminder of IT processing in **local extension racks:**

- TSX 67-20: IT processed by the CPU,
- TSX 87-30: IT processed by the CPU,
- TSX 67-30 and TSX 87-10/20: No IT processing.

(2) Reminder of maximum distances for **remote intelligent modules:**

- TSX 67-20: 750 meters max.,
- TSX 87-30: 1000 meters max.,
- TSX 67-30 and TSX 87-10/20: No remote intelligent modules.