Modicon TSX TIO

QPR Modules

User Manual

870 USE 000 00

03/98

GROUPE SCHNEIDER

■ Merlin Gerin ■ Modicon ■ Square D ■ Telemecanique

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Contents

Symbols, Terminology, Abbreviations

Note: This symbol serves to highlight important facts.

Caution: This symbol points out frequently occurring sources of error.

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Application Note

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Chapter 1
General Specifications

1.1 QPR (Quick Peripheral Response) Overview

The QPR is an I/O module with native intelligence for internal logic operations. The programmable character of its internal logic operations allows the QPR to independently perform logic operations upon its own I/O signals (and INTERBUS directives). The following five different QPR module types exist:

Table 1 QPR module overview

Module	I/O and Interface Complements	Input Delay	Max. No. of Networks
170 QPR 330 00	8 discrete inputs 4 discrete outputs	Typically 0.12 ms	15 networks, thereof max.: 15 logic operation networks 8 up–counter networks 7 timer networks
170 QPR 346 00	16 discrete inputs 12 discrete outputs INTERBUS interface	Typically 0.12 ms	15 networks, thereof max.: 15 logic operation networks 8 up–counter networks 7 timer networks
170 QPR 346 10	16 discrete inputs 12 discrete outputs INTERBUS interface	Typ. 0.055 ms	15 networks, thereof max.: 15 logic operation networks 8 up–counter networks 7 timer networks
170 QPR 346 20	16 discrete inputs 12 discrete outputs INTERBUS interface	Typically 0.12 ms	50 networks, thereof max.: 50 logic operation networks 8 up–counter networks 7 timer networks
170 QPR 346 21	16 discrete inputs 12 discrete outputs INTERBUS interface	Typically 0.12 ms	50 networks, thereof max.: 50 logic operation networks 4 up–counter networks 4 up/down–counters 7 timer networks

In combination with an INTERBUS interface the QPR behaves like an intelligent remote I/O module.

The QPR’s integrated logic operation capability allows the implementation of interlock circuits which remain active even after a system bus failure.

Logic operations can be executed locally in the QPR and guarantee a quick reaction to the process for time–critical applications (no delays caused by the system bus or the PLC user program).

A special switch–off behavior form allows the internal logic operations to only be enabled upon an INTERBUS disturbance. Use can be made of the internal logic operations to act as an emergency program for INTERBUS disturbances, or for the determination of individual output states.

1.2 QPR Block Diagram

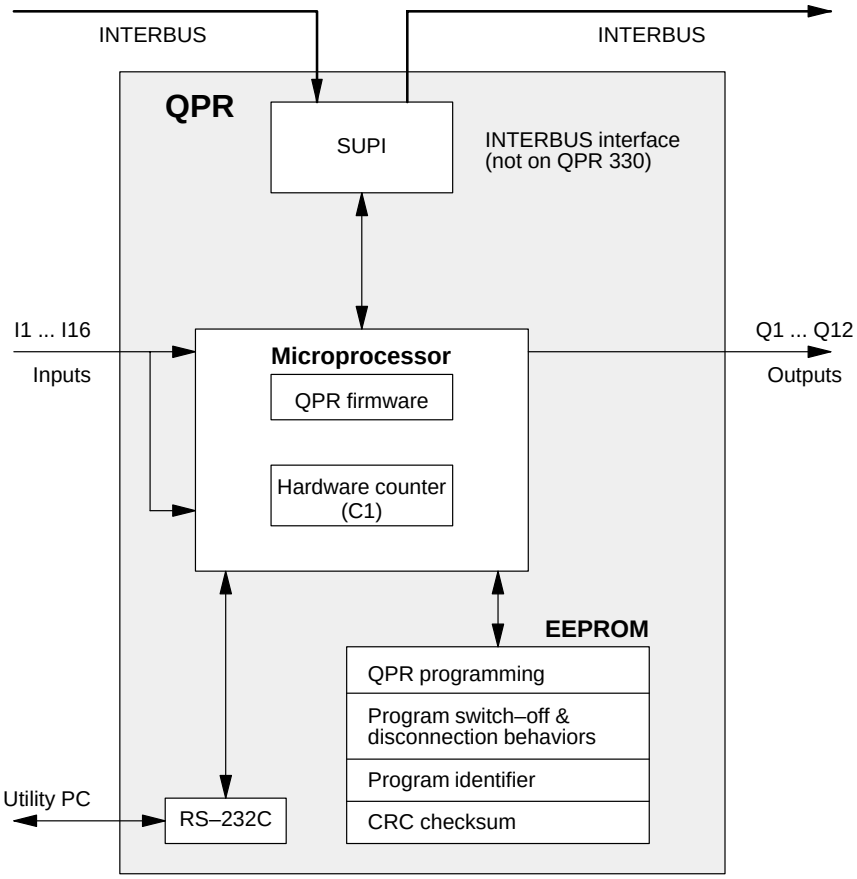

Figure 1 170 QPR 346 00 block diagram

The QPR possesses a serial port for the utility PC to allow internal logic operation programming. Non–volatile program storage is provided by an EEPROM.

At power on the program is loaded from EEPROM and the firmware program interpreter begins cyclic interpretation.

A fast up–counter has been implemented through the connection of process input I1 with the microprocessor's hardware counter.

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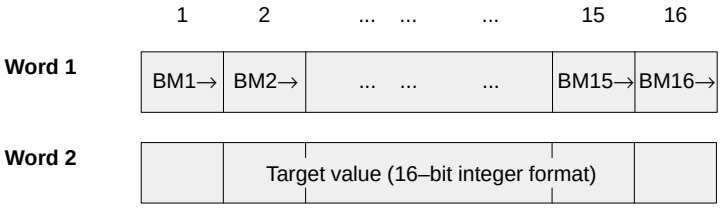
1.3 QPR 346 x0 I/O Data Access

1.3.1 INTERBUS I/O Data Integration

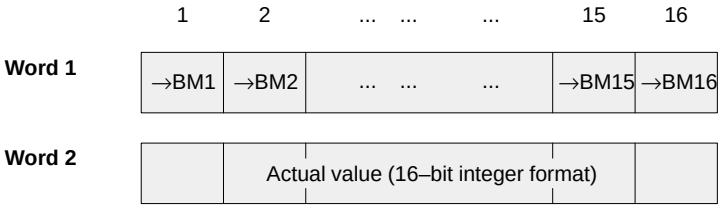
The QPR 346 x0 INTERBUS interface maps to two 16–bit words per transfer direction, which can be sent/received by the INTERBUS master.

INTERBUS Mapping for Bus → QPR Transfer



Explanation	
BM1→, BM2→, ...	Bit from bus master (bit 1 ... bit 16)
Target value	16–bit value, specifying the desired value for a counter or time register

INTERBUS Mapping for QPR → Bus Transfer



Explanation	
→BM1, →BM2, ...	Bit to bus master (bit 1 ... bit 16)
Actual value	16–bit value, giving the current value of a counter or time register

☞ **Note:** Bit 16 is the MSB, bit 1 the LSB.

1.3.2 PLC I/O Data Access

The manner in which QPR 346 I/O data may be accessed with PLC and programming software differs. This section will describe the procedures for the A250, A350/A500 and TSX Quantum.

1.3.2.1 TSX Quantum with NOA 611

The NOA processes the INTERBUS node I/O bits by word and transfers them in accordance with the physical bus sequence of the nodes. It then places the I/O bits into the I/O map 3x– and 4x– references, beginning with the address given as the initial address during the NOA's I/O map entry. This procedure is described in detail in the NOA User Manual (refer to "Associated Documentation" within the foreword section).

Reading QPR Data

The first QPR word containing the "→BM1" ..."→BM16" bits must be converted to a bit string by the user program; the second word containing the actual value can be utilized directly.

Writing Data to the QPR

Whereas the "BM1→" ..."BM16→" bits must be copied into a single word by the user program, the target value can be transferred directly. Pay particular attention that both words have the exact addresses as reserved for the QPR within the I/O map.

1.3.2.2 TSX A250 with BKF 101

The BKF 101 maps INTERBUS nodes to DEP and/or DAP modules. Thus for the QPR a DAP 112 and a DEP 112 must be entered in the A250 component list (pay attention to sequence). Since INTERBUS data is transferred bit–serially, the actual value must be placed into a word before any further processing ("LBW" in the PLC instruction list) and the target value converted to a bit string before transfer ("TBW" in the PLC instruction list).

For the A250 the QPR data can be accessed as follows:

QPR Data	Module	Slot	A250 Address
→BM1, →BM2, ... (bit to bus master)	DEP 112	m (=n+1)	Im.1, Im.2, ..., Im.16
Actual value	DEP 112	m (= n+1)	Im.17 ... Im.32
BM1→, BM2→, ... (bit from bus master)	DAP 112	n	Qn.1, Qn.2, ..., Qn.16
Target value	DAP 112	n	Qn.17 ... Qn.32

1.3.2.3 TSX A250 with BKF 102

The integration of the QPR data within this hardware configuration is possible with the German language ALD program starting with revision 7.2. The QPR must be entered under the menu point ”Direkteingabe” as an ”AM2” with module ID 33_{hex}.

The integration of the QPR data in an AKF program is not possible with the current program revision. A revision corresponding to ALD25 is however in preparation.

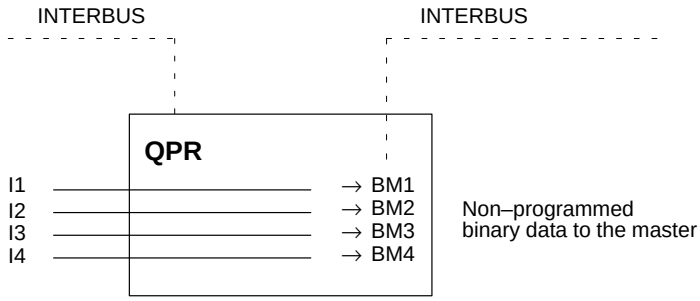
Chapter 2
Programming

2.1 The QPR in the Non–Programmed State

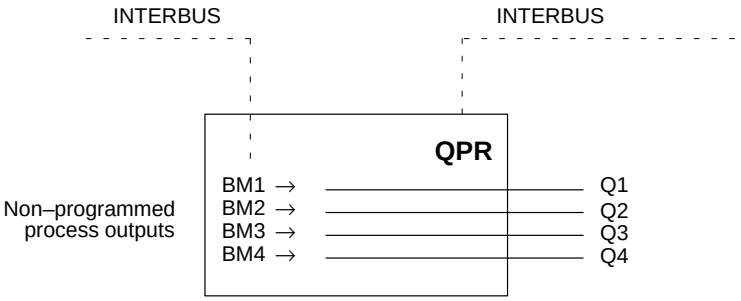
In the non–programmed state (operation list without networks), those QPRs having an INTERBUS interface behave like a remote module (TIO).

In the programmed state (operation list with at least 1 network) the programmed output variables exhibit their programmed behavior; all non–programmed output variables react as would a remote I/O module.

□ All non–programmed binary data transferred from the QPR to the INTERBUS master (→BMx = to bus master), have states identical to the process inputs (Ix).



□ All non–programmed process outputs (Qx) have output states identical to the binary data which was transferred by the INTERBUS master to the QPR (BMx→ = from bus master).



2.2 QPR Programming

QPR programming takes place in 3 steps:

Step 1 Producing a program (beginning with ch. 2.2.1)

Step 2 Converting the program into an operation list (from ch. 2.2.7)

Step 3 Transferring the operation list to the QPR (starting with ch. 2.3)

2.2.1 Applicable Network Structures

Four specific network structures with configurable network elements (NE/Q) are provided for programming purposes.

- □ Logic Operation Network
- □ Up–Counter Network
- □ Up/Down–Counter Network (only for 170 QPR 346 21)
- □ Timer Network

Each network structure possesses 6 network elements serving as input operands (NE1 ... NE6) and a single network element as output operand (Q – not to be confused with the QPR's physical outputs, "Qx").

The sequence of the networks is entirely independent from their processing results, since the signal states of operands and markers don't vary until the beginning of the next processing cycle.

The combinatorial logic operations to be programmed are achieved through an appropriate choice of network elements (NE/Q) from the prescribed network structures.

2.2.2 Logic Operation Network

The logic operation network always exists in the given structural form as shown in the following figure. It consists of an implicit logical OR operation between a branch of 4 logical AND's (NE1–4) and another branch of 2 logical AND's (NE5–6).

All QPR output operands (Qx, →BMx, Mx) are given values through the logic operation network. In addition to direct logical operations between any of the operands, specialized functionality such as flip–flops (RS, D–FF) can be implemented through feedback and the utilization of edge detection operands (refer to the examples in chs. 2.2.2.4 and 2.2.2.3).

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Functionality:

- ☐ Logicical operations upon operands (NE/Q)
- ☐ Realization of flip–flops (RS, D–FF)
- ☐ Driving of output operands (Qx)

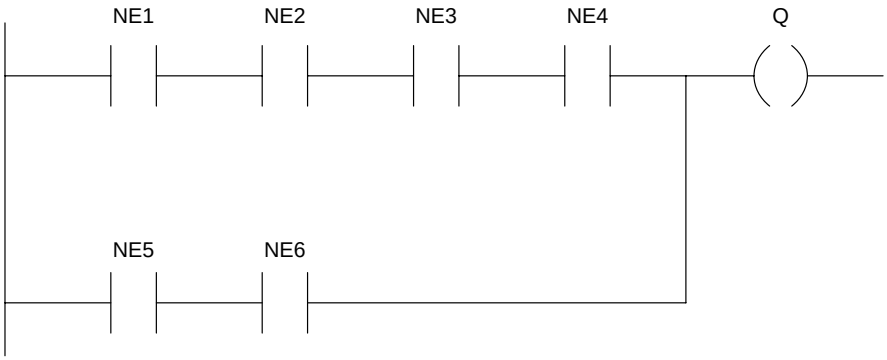
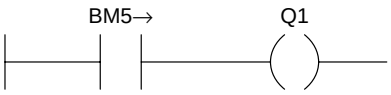


Figure 2 Logic operation network

2.2.2.1 Examples

Here the state of the I1 input is copied to the bit variable →BM5. Pay special attention to the fact that: →BM1 = I1 (implicitly), as long as →BM1 has not been explicitly assigned another input.

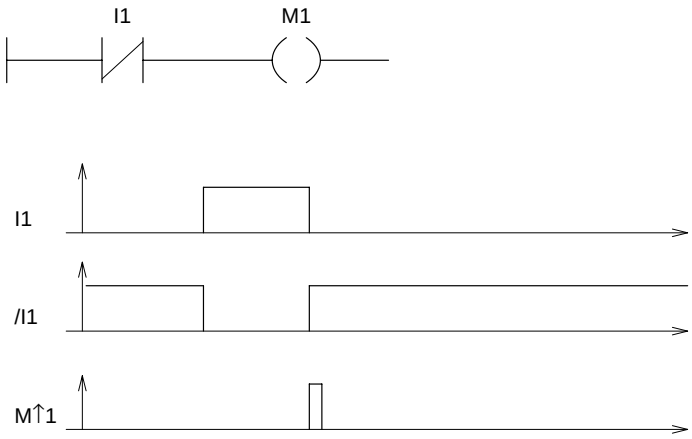


In this example the BM5→ value is assigned directly to the Q1 output. Should Q5 not be used in the QPR program, it will also automatically receive the state of BM5→. Thus the QPR can override the process inputs and outputs through its internal logic operations!

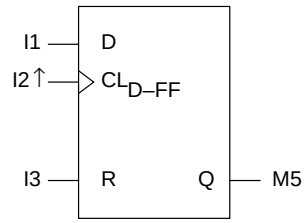
Be certain that a functional assignment of the bit variables Ix/→BMx and BMx→/Qx is made! For example, bit variables which are not to be directly assigned to the hardware outputs should be placed in the BM13→ ... BM16→ range, since these are not mapped to the QPR outputs.

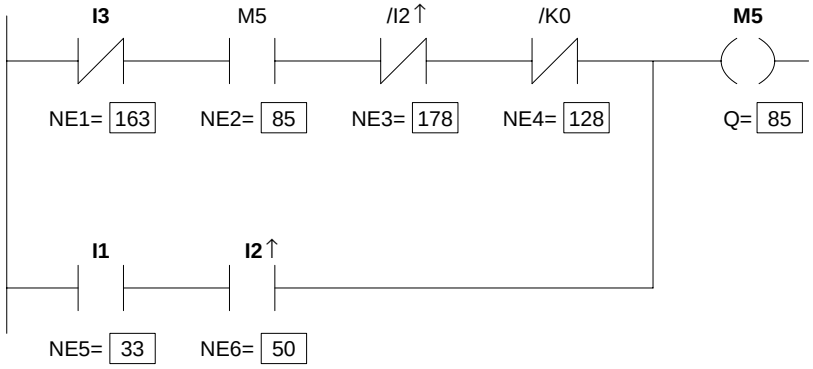
2.2.2.2 Negative edge evaluation example

The following network assigns the negative edge of I1 to M1↑.



2.2.2.3 D flip–flop





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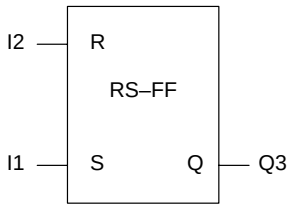
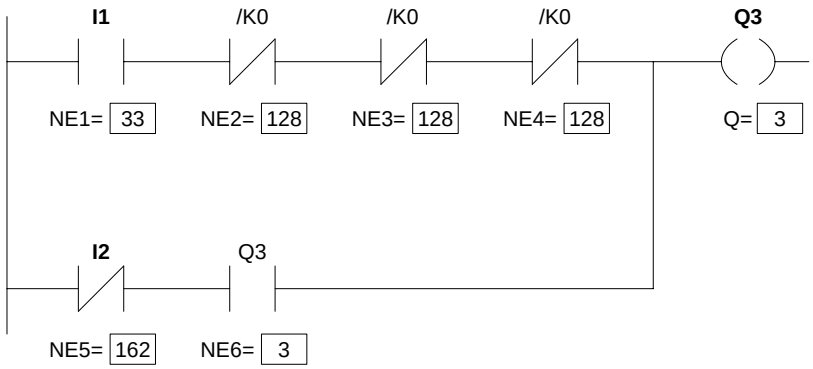
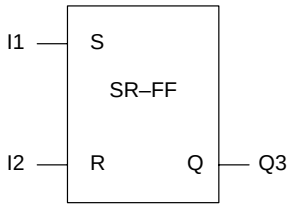
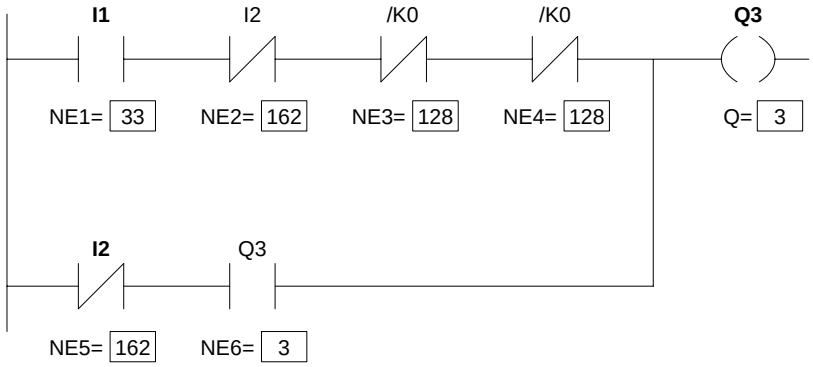
2.2.2.4 RS flip–flop example (set dominant)





2.2.2.5 SR flip–flop example (reset dominant)





2.2.3 Up–Counter Network

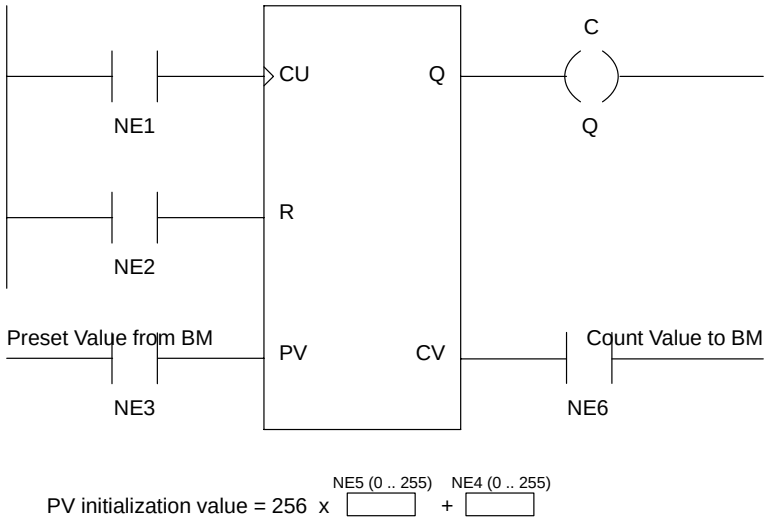


Figure 3 Up–counter network

The up–counter network makes pulse–counting possible. Depending upon the QPR model, up to 8 counters are available, (refer to Table 1 on page 2), whereby counter 1 is a fast hardware counter. Counters have a 16–bit data width, i.e. a maximum counted value of 65535. Should a counted value overflow take place, counting continues from ”0” (”wrap–around”). Only counter operands (C1 ... C8) may be utilized as output operands. Should there be a need to drive process outputs with the Cx operands, they must be applied to a logic operation network.

The counter input is formed by network element NE1; use of the fast counter (C1) requires that it be associated with the process input 1 operand (I1). The counter can be reset to ”0” through the NE2 network element.

The initialization value is coded through two network elements (2 bytes). One network element corresponds to the initialization value low order byte (NE4), the other the high order byte (NE5).

Initialization value = 256 • the NE5 coding + the NE4 coding.

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Example:

Table 2 Initialization value for the counter target value

Initialization Value for the Counter Target Value	NE5 Coding	NE4 Coding
134	0	134
256	1	0
3789	14	205

The counter target value is set to the initialization value at power–up or upon a cold start (see page 29). It can be overwritten by a target value coming from the INTERBUS. This requires that NE3 be assigned with a process input (Ix) or marker bit (BMx→). Transfer takes place when <NE3> = 1. Please note:

- If NE3 is the constant 0, the target value is held at the initialization value
- If NE3 is the constant 1, a new INTERBUS target value is transferred with each cycle
- Should two counters have the same operand assigned to their NE3 network elements, they will both be accepting the same target value

The actual counter value can be transferred to the INTERBUS master with the NE6 network element. NE6 handling is analogous to that of NE3: The current actual value will be transferred to the PLC, when <NE6> = 1 ...

2.2.4 Up/Down–Counter Network (only for 170 QPR 346 21)

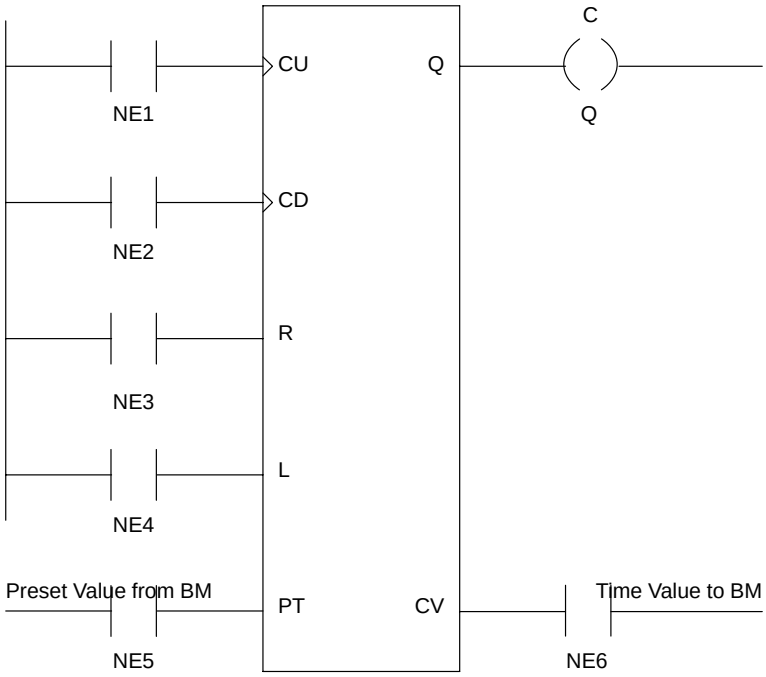

Figure 4 Up/down–counter network

The up/down–counter network makes differential pulse–counting possible with the 170 QPR 346 21. Counters have a 16–bit data width, i.e. a maximum counted value of 65535. Upon counter over/underflow, counting continues with ”wrap around” from ”0” (overflow) or ”65535” (underflow).

A total of 4 up/down–counters are available. The counter operands C5 ... C8 serve as output operands. Should there be a need to drive process outputs with the Cx operands, they must be applied to a logic operation network.

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The network parameters have the following meanings:

Network element	Parameter	Meaning
NE1	CU	Count up counter input (pos. edge).
NE2	CD	Count down counter input (pos. edge).
NE3	R	Reset counted value to ”0” (reset).
NE4	L	Transfer current target value into the actual value (CV = PV).
NE5	PV	Accept the INTERBUS master preset value as counter target value. Contrary to the up–counter, the target value can only be set through the INTERBUS. The counter target value is always set to ”0” at power–up or upon a cold start (page 29). The output is fixed at ”1” until a new non–zero target value is transferred.
NE6	ET	Transfer the actual counter value to the INTERBUS master.
	Q	Counter output. Q = 1: actual value >= target value Q = 0: actual value < target value

2.2.5 On–Delay

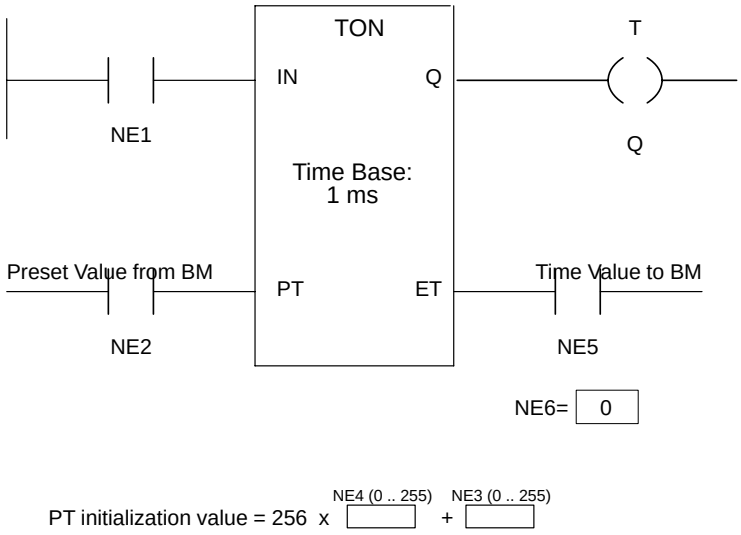

Figure 5 On–delay network

To implement an on–delay timer there are a total of 7 timer networks available. Only timer operands (T1 ... T8) may be utilized as output operands. Should there be a need to drive process outputs with the Tx operands, they must be applied to a logic operation network.

The duration of the delay is calculated from the product of the preset value and the time base (1 ms). With the preset value range from 0 ... 65535 (16–bit), on–delays from 1 ms ... 65535 ms (approx. 1 min.) can be implemented.

The preset value is set to the initialization value at power–up or upon a cold start (see the QPR control commands). It can be overwritten by a preset value coming from the INTERBUS.

The programming of the initialization value and transfer of preset and time values over the INTERBUS corresponds to that of the up–counter (except for the network element numbers).

The NE6 network element is not required and must be coded with the value ”0”.

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2.2.6 Network Coding/Using the Forms

For each network type there exists a corresponding preprinted form, for documentation and operation list preparation, on which the network to be programmed can be depicted. Network elements are first assigned the necessary operands on the form, i.e. the network elements are filled in with the names of the required operands.

The following operands can be utilized as network elements:

Constant 0	K0
Process inputs and outputs	I1, Q4, ...
Markers	M1, M2, ... M16
Binary data from the INTERBUS master	BM1→, BM2→, ... BM16→
Binary data to the INTERBUS master	→BM1 , →BM2, ... →BM16
Process inputs with follow–on edge detection	I1↑, I2↑, ... I16↑
Markers with follow–on edge detection	M1↑, M2↑, ... M16↑
Counters	C1, C2, ... C8
Timers	T1, T2, ... T7
Explicit target/preset values (counter/timer)	0–65535

Positive edges of the corresponding ”I1–I16” and ”M1–M16” operands can be evaluated with the ”I1↑–I16↑” and ”M1↑–M16↑” operands. Marker (”M1–M16”) operands can be usefully applied to combine several networks.

Example The combinatorial logic operations to be programmed: Q1 = I5 & /Q2 & →BM1

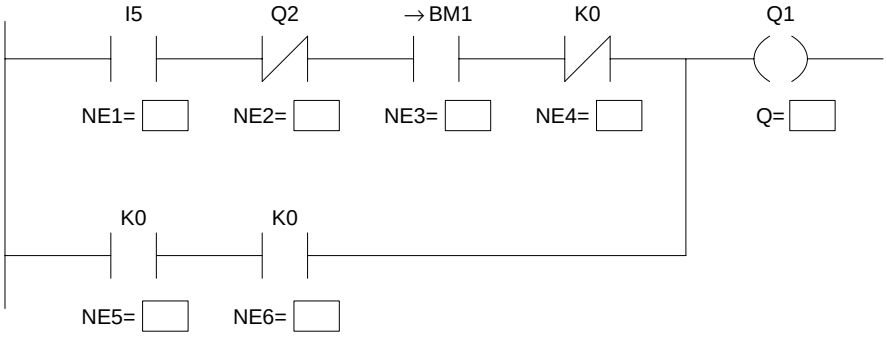

Figure 6 Logic operation network with operands

When the necessary operands have been entered into the network elements on the preprinted form, the actual coding parameters for the individual network elements can be calculated. The coding (0–255) for a network element is

calculated from the sum of the operand addresses (e.g. I5: operand address = 5) and an operand dependent offset.

When using a negated contact (break contact/inverted output) an additional 128 must be added to the sum.

Use of negated contacts for die NE1–6 network elements can be made in every network structure. The actual network output (Q) may only be inverted within the logic operation network.

A table of the operand dependent offsets is provided to simplifiy the coding calculations.

Table 3 Network element coding

	Network Element (NE)	**Address**	**Offset**	**/ (Neg.)**	**= NE**
K 0	Constant 0 (binary ”0” value = ”constant 0”)	0	–	+128	
Q	Output	[1..o]	+0		
BM→	Data from INTERBUS master	[1..16]	+16		
I	Process input	[1..i]	+32		
I↑	Process input with follow–on positive edge detection	[1..i]	+48		
→BM	Data to INTERBUS master	[1..16]	+64		
M	Marker	[1..16]	+80		
M↑	Marker with follow–on positive edge detection	[1..16]	+96		
C	Up–counter	[1..8]	+112		
T	On–delay	[1..7]	+120		

[ ]: max. operand address range
o: max. process output complement
i: max. process input complement

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The following figure shows the example network with network elements coded.

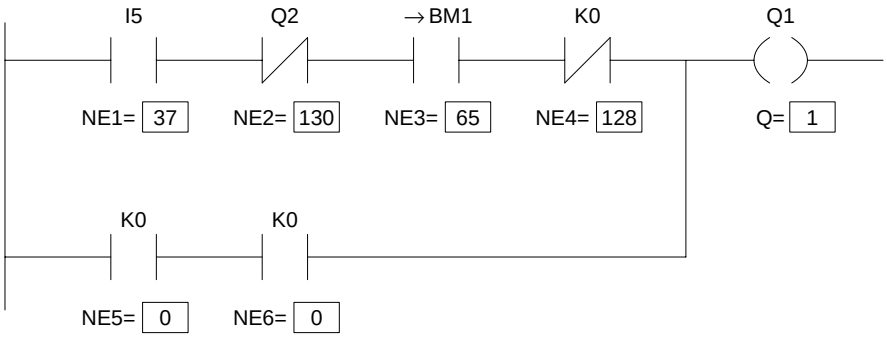


Figure 7 Logic operation network with operands and their codings

Network elements (NE1–6) not required in a network structure can be deactivated with the constant 0 (= ”K0”) operand. However a hard connection can be easily achieved with a negated contact (break contact). In the example network the lower branch was not required and hence deactivated through the use of ”K0” operands (NE5, NE6). The NE4 network element not required in the upper branch was, in contrast, bridged with a ”K0” operand and a negated contact (hard connection).

2.2.7 Operation List Structure

The QPR operation list consists of coding sequences for the individual networks and additional administrative information.

Table 4 Operation list structure

List Element No.	List Element	Meaning
1	STX	Operation list start
2	PIaaa	Program identifier (”aaa” is freely definable)
3	Kbb	Control word (switch–off/disconnection behavior)
4	KOP (or LD)	Ladder diagram
5	Ncc	Network no. (ascending) cc = 1 .. 50 for 170 QPR 346 20, cc = 1 .. 15 otherwise
6	ccc	Q parameter
7	ccc	NE1 parameter
8	ccc	NE2 parameter
9	ccc	NE3 parameter
10	ccc	NE4 parameter
11	ccc	NE5 parameter
12	ccc	NE6 parameter
....	Repetition of list elements 5 – 12	Next network
Last entry	ETX	Operation list end

The individual list elements consist of ASCII character sequences (e.g. ”STX”), whereby no case differentiation is made.

The valid separators listed in the following table may be used for the separation of individual character strings:

Table 5 Separators

Separators	Decimal ASCII Code
Horizontal Tabulator (HT)	9
Linefeed (LF)	10
Vertical Tabulator (VT)	11
Formfeed (FF)	12
Carriage Return (CR)	13
Space (SP)	32

Additional commentary text can be inserted in the operation list with a semicolon (”;”). All the following characters up to the end of line (”CR”) are interpreted as commentary.

The operation list header begins with the ”STX” start symbol and consists of the following elements:

□ Program Identification
As an aid to individual program naming, the last 3 positions of the 5–place program identifier (”PIaaa”) may be filled with any alphanumeric characters (”A–Z”, ”0–9”, ”_”).

□ Control Word
The QPR’s switch–off/disconnection behavior is determined through the control word (cp. 2.2.8).

□ Network Representation for the Form
Marks the type of programming representation for the forms used.

Directly after the operation list header follow the parameters of the individual networks and the ”ETX” end symbol.

Every network consists of a network number and 7 parameters for the network elements (NE/Q). The network number is to be stated as a character string consisting of an ”N” and a 1– or 2–digit decimal number (leading zeros are allowed).

The network numbers must be given in ascending order (beginning with N1). Depending upon the type of QPR, either 15 or 50 networks are allowed (refer to Table 1).

State the parameters for the network elements (NE/Q) as 1–3 digit decimal numbers (leading zeros are allowed).

Following the parameters of the employed networks the operation list must be terminated with the ”ETX” end symbol.

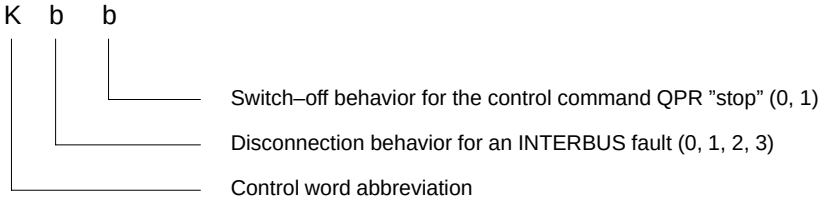
☞ **Note:** Should the operation list only consist of the operation list header and the end symbol, the QPR will be in the non–programmed state (behavior as for a remote I/O module).

When an output operand is repeatedly programmed, its use in the network with the highest network number dominates.

2.2.8 QPR Switch–Off/Disconnection Behavior

The switch–off/disconnection behavior of the QPR must be determined through a control word (Kbb) in the operation list.

The control word consists of 3 characters.



Disconnection behavior for an INTERBUS fault (communication between the QPR and INTERBUS master is interrupted)

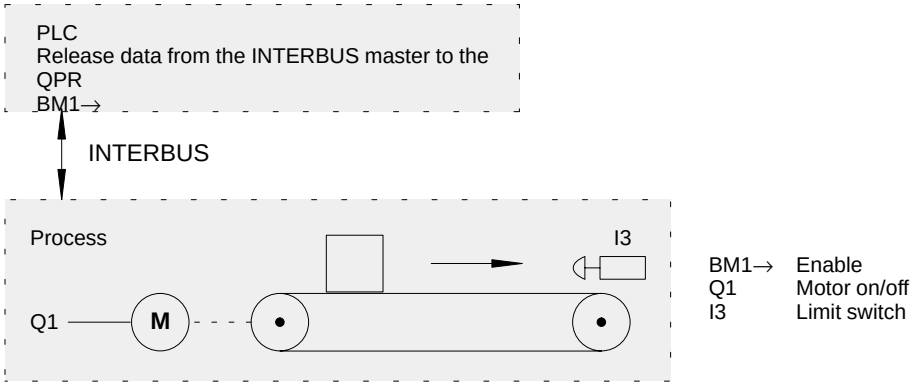
0		The QPR is not equipped with an INTERBUS interface
1	Halt internal logic operations	All QPR outputs and data from the INTERBUS master (BM”) are set to ”0”
2	Internal logic operations remain active	All data from the INTERBUS master are set to ”0”. Only those counters and on–delays, whose network elements NE3 resp. NE4 are assigned to marker bits, will continue to function with the last valid target/preset values.
3	Only activate the internal logic operations after an INTERBUS disturbance (during correct INTERBUS operation the QPR behaves like a TIO module).	At the beginning of internal logic operations the following initialization is carried out: □ All data from the INTERBUS master to the QPR = 0 (integer data: target/preset values from BM; binary data: BM→) □ All markers (M, M↑), on–delays (T), counters (C), process outputs (Q) and associated actual values of the on–delays, resp. counters = 0

Switch–off behavior for the control command QPR ”stop” (halt of internal logic operations)

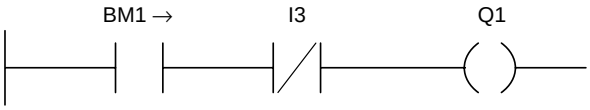
0	All QPR outputs and data from the INTERBUS master (BM”) are set to ”0”.
1	All QPR outputs and data from the INTERBUS master (BM”) are retained.

2.2.9 Programming Example

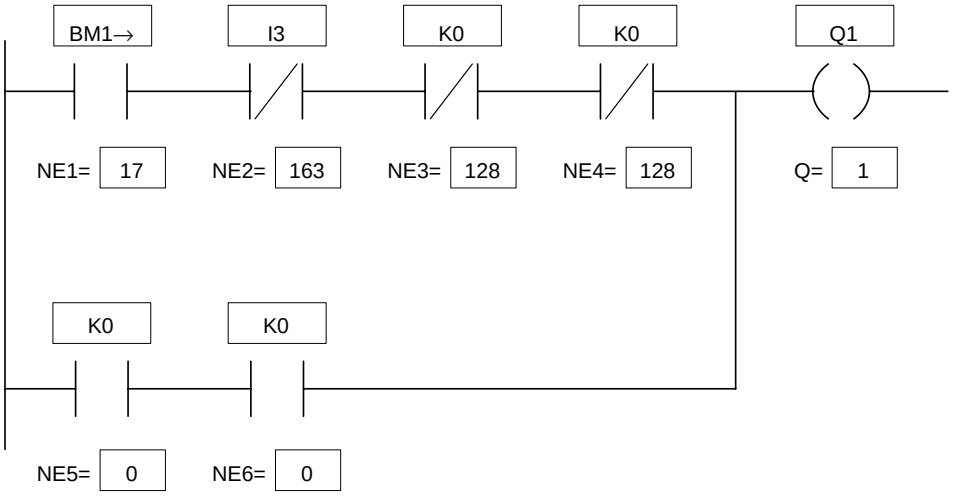
Transport goods on a conveyor belt with enabling and limit switches



The network to be programmed is



Logic operation network form



Operation List

```
            ;Transport goods on the conveyor belt
            ;any further commentary could go here
            ;....
STX         ;Operation list start
PI123       ;Program identifier: 123
K20         ;Disconnection behavior for failure: internal logic
KOP         operations remain active
N1          ;Ladder diagram
1           ;Network no. 1
17          ;Q = Q1
163         ;NE1 = BM1→, Conveyor belt enable from the PLC
128         ;NE2 = /I3, Conveyor belt limit switch not reached
128         ;NE3 = 1, constant ”1”
0           ;NE4 = 1, constant ”1”
0           ;NE5 = 0, constant ”0”
ETX         ;NE6 = 0, constant ”0”
            ;Operation list end
```


Breite: 185 mm
Höhe: 230 mm

2.3 Producing and Transferring the Operation List under MS–DOS

QPR programming is achieved through the transfer of an ASCII character string (operation list) to the QPR's serial port for the utility PC. During the transfer the QPR performs an examination of the operation list. The QPR "RUN" status LED displays the transfer status after operation list transfer completion:

LED is off	Operation list ok
LED flashing	There is an error in the operation list or there is no valid operation list present

Should an error have been determined in the operation list, information about the type of error and the operation list error line can be provided through the QPR status readout control command (refer to page 27, ch. 2.4.1.1).

Preparation of the operation list can be performed with any conventional ASCII editor or text system which provides an ASCII output format.

Step 1 Editing of the operation list with a text editor, for example with the editor provided with MS–DOS, "edit.exe".

Step 2 Saving the operation list as a text file.

Step 3 Configuring the PC's serial port (e.g. COM1) with the MS–DOS "MODE" command.

Example: C:\>mode com1:96,e,8,1

Step 4 Copying the text file to the serial port (e.g. COM1) with the MS–DOS "COPY" command.

Example: C:\>copy pro_list.txt com1

Step 5 The QPR "RUN" status LED displays the transfer status:

Off: Operation list transfer successful
Flashing: Operation list or transfer fault

☞ **Note:** Transfer of a flawless operation list overwrites the operation list previously resident on the QPR. Operation list transfer may take place during any QPR state (RUN; STOP; or when no operation list is present).

2.4 Use of Terminal Programs

In addition to a menu–assisted transfer of operation lists, terminal programs permit the use of simple diagnosis and control commands.

In response to the transfer of an operation list or control command, the QPR sends back ASCII text format information over the serial port for the utility PC, which can be displayed by the terminal program as text, or stored as a file.

2.4.1 QPR Control Commands

The QPR control commands can be entered over the keyboard with a terminal program as normal ASCII text (e.g. ”status”, ”stop”, ...). Should the QPR receive an inconsistent character string, it ignores the received sequence and acknowledges by sending a ”carriage return” (”CR”) and two ”linefeeds” (”LF”).

2.4.1.1 QPR Status Readout (”status”)

After the QPR receives the ”status” character string it produces a QPR status report. This status report readout has the following format:

STX	Start symbol
<nnn>	Type identifier, refer to the next page
F:nn	Error no., refer to the next page
Z:nn	nn = the operation list error line in which the error occurred (this line is only output in the event of an error!)
S:bbbbbb	Status information, refer to the following page
ETX	End symbol

Type Identifier The type identifier is a 3–digit code for identification of the QPR types.

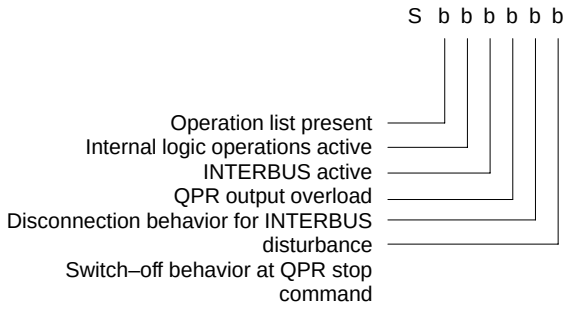
Type Identifier	QPR Type	Properties
001	170 QPR 346 00 170 QPR 346 10 (fast processor)	16 inputs, 12 outputs INTERBUS interface
004	170 QPR 330 00	8 inputs, 4 outputs
101	170 QPR 346 20	16 inputs, 12 outputs INTERBUS interface
201	170 QPR 346 21 (up/down–counter)	16 inputs, 12 outputs INTERBUS interface

Error No. Should an error occur during operation list transfer or program load from EEPROM, the source of error is coded in the error number.

Error No.	Source of Error
0	No error
1	Parity error
2	Unexpected character
3	Invalid network operand (NE1–6) coding
4	Invalid coding for INTERBUS disconnection behavior
5	Invalid coding for switch–off behavior at QPR stop command
6	Unexpected network no.
7	Max. number of networks exceeded
8	Invalid coding (> 255)
9	CRC error during EEPROM readout
10	Neg. output operand (Q) in counter or timer network
11	Invalid output operand (Q) coding

Error Line Should an error occur during the operation list transfer, the line number of the faulty line is declared.

Status Information Example S:111020
Operation list present, internal logic operations active, INTERBUS active, no QPR output overload, internal logic operations remain active upon bus interruption, QPR outputs and BM data = 0 at the QPR stop command.



2.4.1.2 QPR Stop (”stop”)

Functionality:

- □ Halts QPR internal logic operations
- □ Outputs QPR status (see ”status”)

2.4.1.3 QPR Warm Restart (”wstart”)

Functionality (only when the QPR internal logic operations are halted):

- □ Activate QPR internal logic operations, whereby the last data image (containing all markers, timers, counters) previous to the halt is used
- □ Outputs QPR status (see ”status”)

2.4.1.4 QPR Cold Start (”nstart”)

Functionality (only when the QPR internal logic operations are halted):

- □ Activates QPR internal logic operations with an initialized data image

  Initialization:
  - □ All data from the INTERBUS master to the QPR = 0 (integer data: target/preset values from BM; binary data: BM→
  - □ All markers (M, M↑), on–delays (T), counters (C), process outputs (Q – not NE/Q!) and associated actual values of the on–delays, resp. counters = 0

- □ Outputs QPR status (see ”status”)

2.4.1.5 List the QPR operation list (”list”)

Functionality: #Outputs the operation list in a standardized format (no commentary or capitals)

Breite: 185 mm
Höhe: 230 mm

2.4.2 ”Norton Commander” Terminal Program ”Term90” (MS–DOS)

2.4.2.1 Settings

The ”Term90” terminal program can be started from within ”Norton Commander” in the ”Commands” menu, with command ”Terminal”.

The following settings should be made:

Menu entry	Settings
”Settings”	Activate option ”Echo”
”Ports”	Port: chose the port to be employed (e.g. COM1) Baud Rate: 9600 Data bits: 8 Parity: Even Stop bits: 1 bit Handshake: leave as default
”Terminal Emulation”	Option: VT100

2.4.2.2 Transfer operation list to the QPR

Menu `File` → Menu entry `Send` → Submenu entry `ASCII` → select ASCII text file (operation list) and acknowledge ([OK]).

2.4.2.3 Readout the operation list and store in an ASCII text file

Step 1 Open the file in which the operation list is to be saved.

Menu `File` → Menu entry `Log file` → Enter the file name and acknowledge ([OK]).

Step 2 Readout the QPR operation list

Enter the (ASCII) character string ”list” through the keyboard

Step 3 Save the ASCII text file (containing the operation list)

Menu `File` → Option `Log file` close.

2.4.2.4 Exit ”Term90”

Menu `File` → Menu entry `Exit.`

2.4.3 Windows Terminal Program ”Terminal”

2.4.3.1 Settings

The terminal program ”Terminal” is included in the Windows 3.1/3.11 program package within the ”Accessories” program group.

The following settings are required:

Menu	Menu entry	Settings
”Settings”	Terminal Emulation...	Option DEC VT–100 (ANSI)
	Terminal Preferences...	Terminal modes: local echo selected, line wrap deselected CR→CR/LF: outbound selected
	Text Transfers...	Flow control: Standard Flow Control selected
	Communications...	Baud Rate: 9600 Data Bits: 8 Stop Bits: 1 Parity: Even Flow Control: None Parity Check: selected Connector: chose the port to be employed (e.g. COM1)

In order to achieve the declared configuration settings, it may be necessary to go through the following configuration sequence:

1. Data bits: 7
2. Parity: Even
3. Stop Bits: 2
4. Data bits: 8
5. Stop Bits: 1

Terminal program settings can be saved in a terminal file (extension .trm) and restored through a file open.

2.4.3.2 Transfer operation list to the QPR

Menu `Transfers` → Menu entry `Send Text File...` → select ASCII text file (operation list) and acknowledge (OK).

2.4.3.3 Readout the operation list and store in an ASCII text file

Step 1 Open the file in which the operation list is to be saved.

Menu `Transfers` → Menu entry `Receive Text File...` → enter ASCII text file name and acknowledge (OK).

Step 2 Readout the QPR operation list

Enter the (ASCII) character string ”list” through the keyboard

Step 3 Save the ASCII text file (containing the operation list)

Press the `Stop` button at the bottom of the window.

2.4.4 Windows ’95 Terminal Program ”HyperTerminal”

2.4.4.1 Settings

The terminal program ”HyperTerminal” is included in the Windows ’95 program package within the ”Accessories” program group.

After ”HyperTerminal” has been started a name and icon for the connection can be chosen, saving the settings made. Upon a renewed ”HyperTerminal” start through the icon, the saved settings will be applied. Several of the settings listed below can be entered directly in the ”HyperTerminal” start dialog.

The following settings are required:

Menu	Menu entry	Register	Settings
File	Properties	Phone Number	Connect Using: Direct to COM1 (or COM2)
		Submenu: Configure...	Bits per second: 9600 Data bits: 8 Parity: Even Stop bits: 1 Flow control: None
		Settings	Emulation: VT100
		Submenu: ASCII Setup...	Select Option: Echo typed characters locally

2.4.4.2 Transfer operation list to the QPR

Menu `Transfer` –> Menu entry `Send Text file...` –> select ASCII text file (operation list) and acknowledge (OK).

2.4.4.3 Readout the operation list and store in an ASCII text file

Proceed as follows:

Step 1 Open the file in which the operation list is to be saved

Menu `Transfer` –> Menu entry `Capture Text...` –> enter ASCII text file name and acknowledge

Step 2 Readout the QPR operation list

Enter the (ASCII) character string ”list” through the keyboard

Step 3 Save the ASCII text file (containing the operation list)

Menu `Transfer` –> Menu entry `Capture Text...` –> Submenu `Stop`

Breite: 185 mm
Höhe: 230 mm

34 Programming

Appendix A
Module Descriptions

Breite: 185 mm
Höhe: 230 mm

36 Module Descriptions

170 QPR 330 00
QPR Module w/o INTERBUS Interface

The QPR 330 is an I/O module with native intelligence for internal logic operations.

Enclosed you will find the following module specific information:

- ☐ Features and Functional Details
- ☐ Configuration
- ☐ Diagnosis
- ☐ Technical Specifications

Width: 185 mm
Height: 230 mm

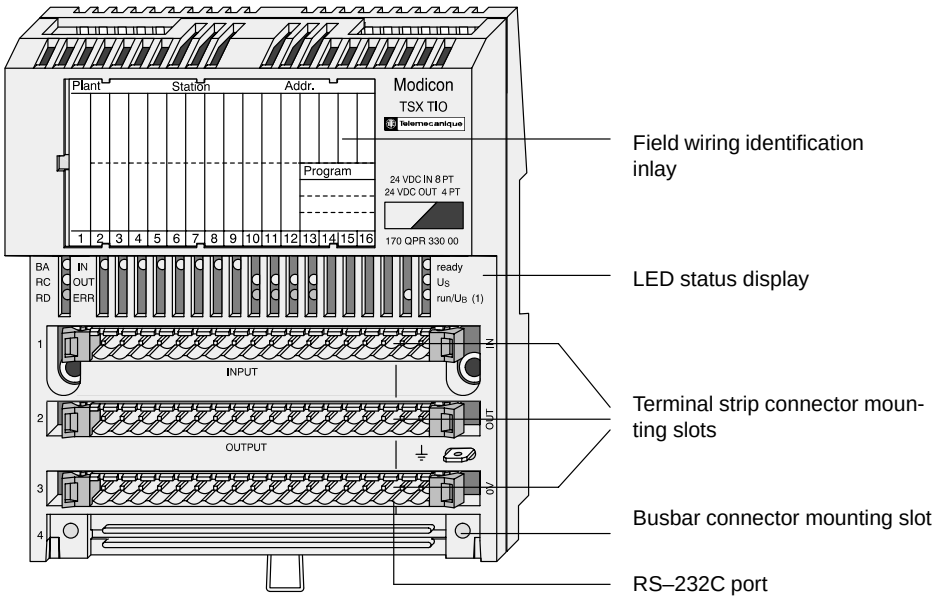


Figure 8 Front view

The QPR 330 is an I/O module with native intelligence to perform logic operations upon it's process I/O signals. It does not possess a bus connection and can thus only operate in stand–alone mode.

It is equipped with 8 discrete inputs and 4 discrete outputs for 24 VDC. Inputs and outputs are equipotential. The proximity switches (2-, 3-, or 4-wire) and actuators (2-, 3-wire) can be connected directly to the module terminal strips without the need for external distribution blocks.

Outputs are electronically short circuit and overload–proofed. In the case of a short circuit or overload the temperature of the corresponding output driver increases, which then causes the output to be switched off. After the component temperature has dropped below it's restoration threshold the output is reactivated. This procedure repeats in its entirety until the overload cause is eliminated.

2 Configuration

- ☐ Module Installation
- ☐ Programming Device Connection (RS–232C Port)
- ☐ Terminal Block Coding and Installation
- ☐ Input and Output Wiring

2.1 Module Installation

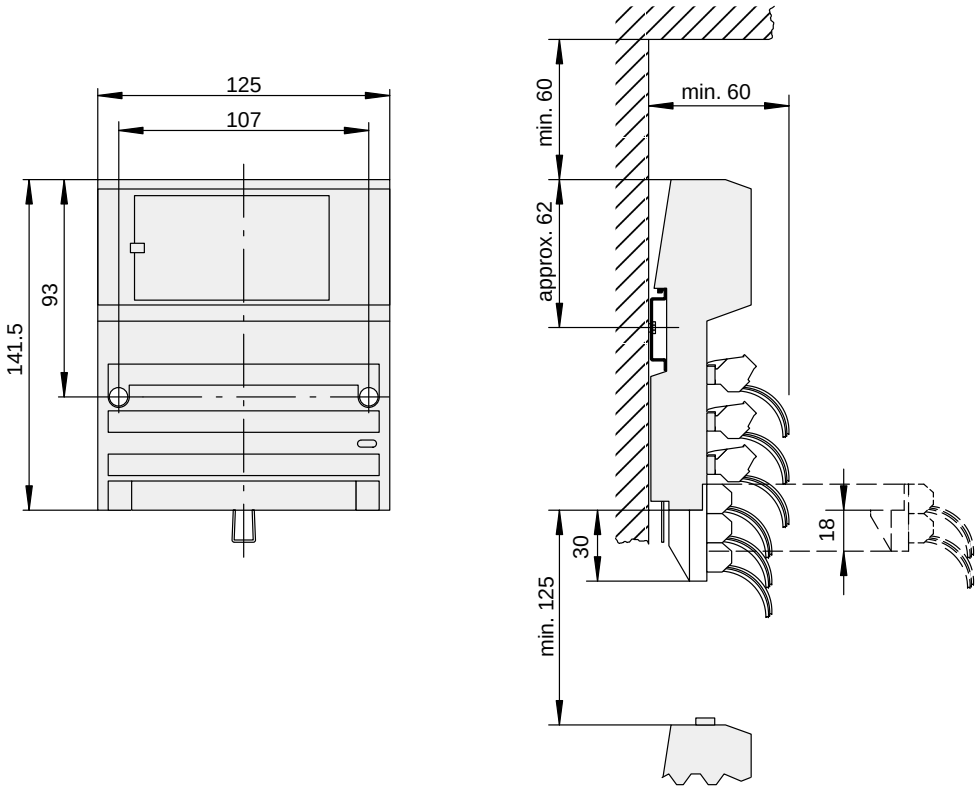


Figure 9 Module dimension drawing

Width: 185 mm
Height: 230 mm

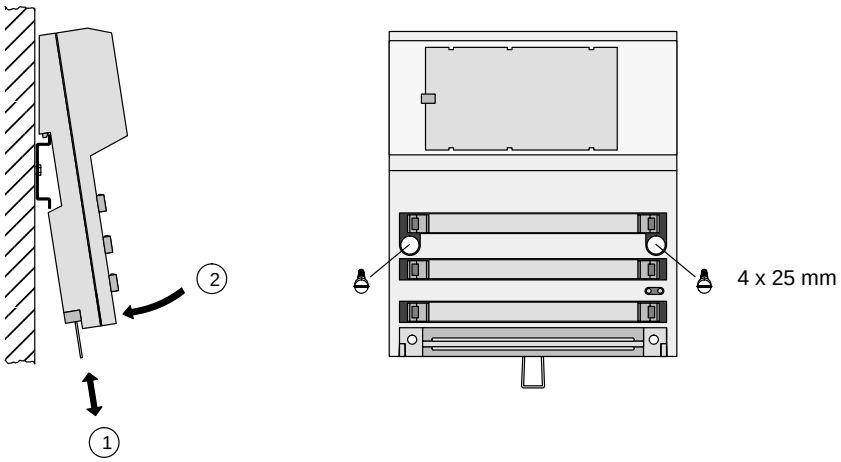


Figure 10 Module installation on a mounting rail (left) and on a wall (right)

2.2 Programming Device Connection

The RS–232C programming device port signals appear on terminals 13 ... 16 of the row 3 terminal strip. Cable 170 NAA 060 00 should be used for the programming device connection.

Terminal	Signal	Function
3.13	D1 (TXD)	Transmitted data
3.14	E2 (GND)	Signal ground
3.15	D2 (RXD)	Received data
3.16		Cable shielding

2.3 Terminal Block Coding and Installation

2.3.1 Terminal Style Selection

The connection of I/O peripherals and the module supply is accomplished through three 18–pole terminal blocks. These are available as a 3–piece set in two variations:

- □ Screw–in terminals, for cable cross sections up to 2.5 mm^2
- □ Spring tension terminals, for cable cross sections up to 1.5 mm^2

Depending upon the specific wiring and the sensor/actuator selection, a 1–, 2–, or 3–row busbar may be required. These are available individually in screw–in and spring tension variants.

2.3.2 Safety Coding

The module may be employed in the safe voltage range (< 42.4 VAC / < 60 VDC). Safety coding prevents that terminal blocks which are wired for the hazardous voltage range can be inadvertently mounted on the module.

Thus the module is delivered with previously coded pin connectors. It lies in the responsibility of the user to code the terminal blocks (not coded at the factory).

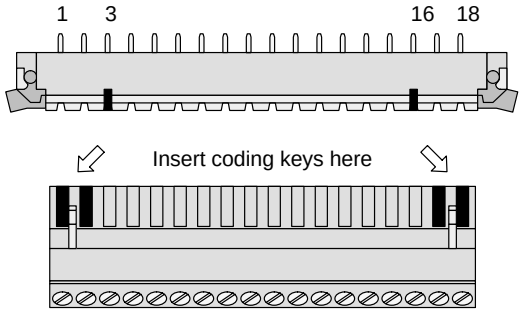


Figure 1 Safety coding demonstrated on the screw–in terminal block

2.3.3 Individual Coding

The user may still undertake an individual coding of the remaining, free coding positions, so as to block–out connectors of the same module types from one another. However, this must not under any circumstances cancel out or alter the safety coding.

2.3.4 Terminal Block Mounting, Removal

To mount terminal blocks, simply press them in pin connectors precoded for 24 VAC (module rows 1 ... 3). To loosen the terminal block press both extractors.

Tightly screw the busbar to the the module’s row 4.

Width: 185 mm
Height: 230 mm

2.4 Input and Output Wiring

The following voltages must be supplied externally (refer to the connection schemes):

- ☐ UB to supply the internal logic (row 1, terminal 18)
- ☐ UB1 to supply the inputs (row 3, terminal 17 or 18)
- ☐ US1 to supply the outputs (row 2, terminal 18)

The terminals in busbar rows 4 ... 6 are row–common, but without any connection to the module logic. Different applications will require 1–, 2–, or 3–row busbars.

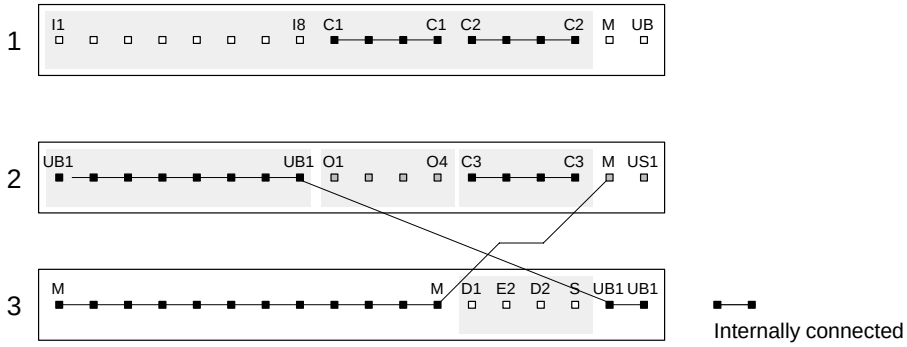


Figure 11 QPR connection mapping

2.4.1 Basic Requirements

The following basic guidelines should be respected:

- ☐ Load factor data must be in accordance with the listed technical data.
- ☐ When use is made of an unregulated 24 VDC power supply, the QPR should be protected through the use of an appropriate overvoltage protection (e.g. OVP 001).
- ☐ Outputs of inductive loads require an on–site (parallel to the operating coil) protective circuit with clamping/suppressor diode, when switching components are resident in the output lines, or the lines to the peripherals are very long.
- ☐ Fusing should be dimensioned to match the total current of the connected consumers, but not to exceed 4 A fast–blow for the inputs or 8 A fast–blow for outputs.

2.4.2 Wiring Examples

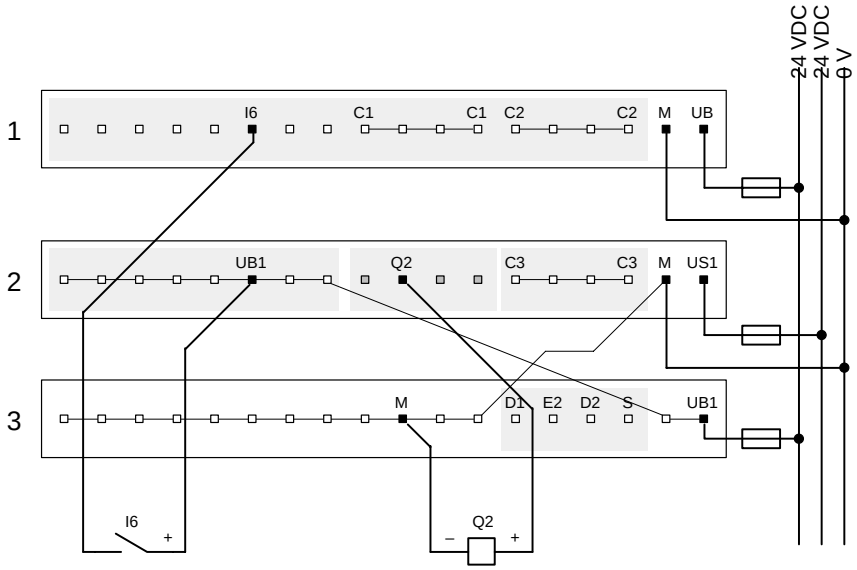


Figure 12 Component selection with 2–wire switching device (push–button/switch) and 2–wire actuator

Width: 185 mm
Height: 230 mm

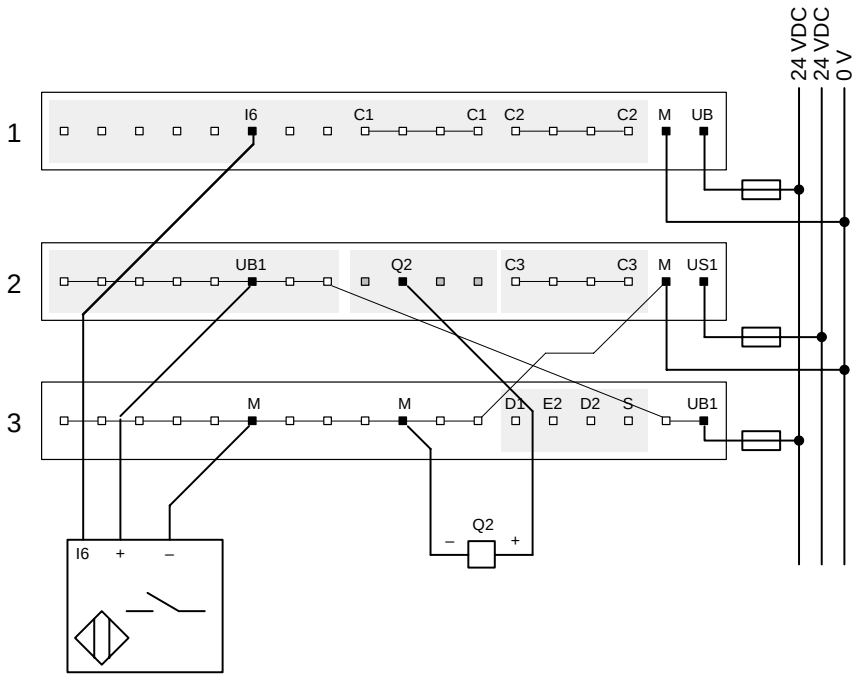


Figure 13 Component selection with 3-wire proximity switch and 2-wire actuator

☞ **Note:** The connection of 4–wire sensors requires the 1–row busbar for PE distribution.

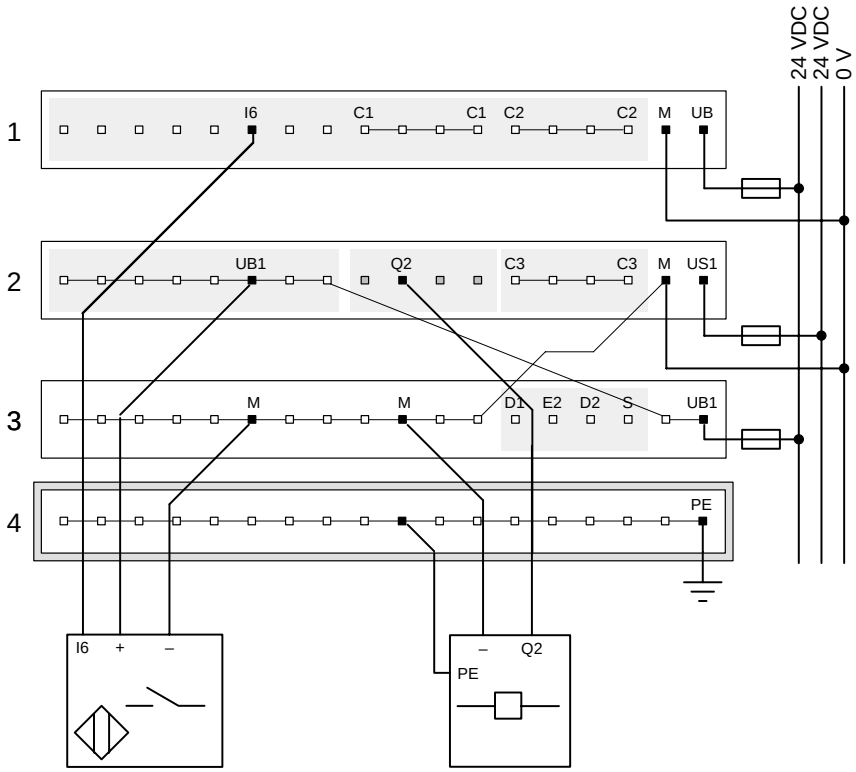


Figure 14 Component selection with 3-wire proximity switch and 3-wire actuator

Width: 185 mm
Height: 230 mm

3 Diagnosis

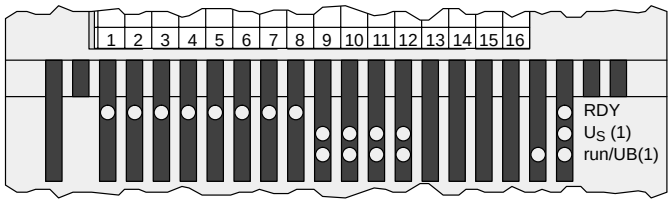


Figure 15 QPR 330 LED status display arrangement

LED	Status	Function
RDY	Green	Ready for service; UB supply voltage for internal logic within tolerance and module not in reset.
	Off	Not ready; UB supply voltage for internal logic not within tolerance or module in reset.
US1	Green	US1 output voltage is present.
	Off	US1 output voltage is not present. Check the US1 source.
UB1	Green	UB1 input voltage is present.
run	Green	A valid operation list is present and internal logic operations active
	Flashing	An operation list is faulty or not present, or the transfer was disturbed
	Off	A valid operation list is present and internal logic operations halted
1 ... 8 Upper row	Green	Input status (an LED per input); input point active, i.e. input carries ”1” signal (logically ”ON”).
9 ... 12 Middle row	Green	Output status (an LED per output); output point active, i.e. output carries ”1” signal (logically ”ON”).
9 ... 12 Bottom row	Red	Output overload (an LED per output); short circuit or overload on the corresponding output.

4 Technical Specifications

Assignment

Node	Does not possess a bus connection
Installation	Mounting rail, or alternatively mounting to a wall or machine housing

Module Voltage Supply

Supply voltage	UB = 24 VDC
Current consumption	Typically 70 mA.
Reference potential	M

Process Interface

Inputs	
Sensor supply	UB1 = 24 VDC
Reference potential	M
Complement	8 type 1+ inputs
Rated signal value	24 VDC
Signal levels	”1” signal +11 ... 30 VDC ”0” signal –3 ... +5 VDC
Input current	6 mA for 24 VDC
Input delay	Typically 0.12 ms
External fusing	Max. 4 A (fast–blow)
Outputs	
Working voltage	US1 = 24 VDC
Reference potential	M
Complement	4 solid–state outputs
Style	Protected against short circuits and overloads
External fusing	Max. 4 A (fast–blow)
Switched current at max. 60 ^{o}C	Max. 0.5 A per output 2 A per module
Resistive load	12 W per output
Inductive load	12 W per output
Bulb load	1.2 W per output
Switching cycle	Inductive load (0.5 A) 1000/h resistive load (0.5 A) 100/s bulb load (1.2 W) 8/s

Width: 185 mm
Height: 230 mm

Potential Relationships

Equipotential	UB, UB1, US1 to another

Mechanical Design

Module	In standard housing
Dimensions (W x H x D)	125 x 142 x 44 mm
Weight	260 g

Process Connection Styles

Rows 1 ... 3	Plugable terminal blocks with screw–in or spring tension terminals
Row 4	Threaded busbar with screw–in or spring tension terminals

Environmental Conditions

Regulations	Meets VDE 0160, UL 508
Safety classification	IP20
Ventilation	Module hanging, natural convection
Ambient temperature	0...60°C
Power dissipation	Typically 4 W

170 QPR 346 00, ...
170 QPR 346 21
TIO Modules with Internal Logic Operations

The 170 QPR 346 XX is an INTERBUS node with native intelligence for internal logic operations.

Enclosed you will find the following module specific information:

- ☐ Features and Functional Details
- ☐ Configuration
- ☐ Diagnosis
- ☐ Technical Specifications

Width: 185 mm
Height: 230 mm

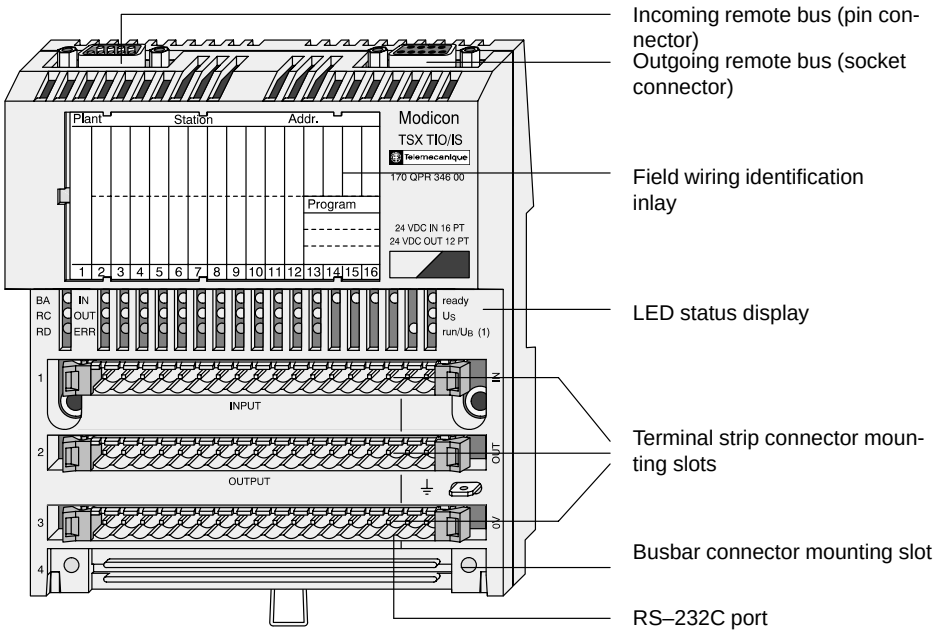


Figure 16 Front view

The QPR 346 XX is an INTERBUS I/O module with native intelligence to perform logic operations upon it's I/O signals and INTERBUS directives. It is equipped with 16 discrete inputs and 12 discrete outputs for 24 VDC. The proximity switches (2-, 3-, or 4-wire) and actuators (2-, 3-wire) can be connected directly to the module terminal strips without the need for external distribution blocks.

Inputs and outputs are equipotential. The incoming remote bus signals are galvanically isolated from the remaining logic by optical couplers.

Outputs are electronically short circuit and overload–proofed. In the case of a short circuit or overload the temperature of the corresponding output driver increases, which then causes the output to be switched off. After the component temperature has dropped below it's restoration threshold the output is reactivated. This procedure repeats in its entirety until the overload cause is eliminated.

For a short circuit or overload the error LED assigned to the output lights and the module reports a "Module Error" to the bus master. This signal can be analyzed for example, within a user program.

2 Configuration

- ☐ Module Installation
- ☐ INTERBUS Connection
- ☐ Programming Device Connection (RS–232C Port)
- ☐ Terminal Block Coding and Installation
- ☐ Input and Output Wiring

2.1 Module Installation

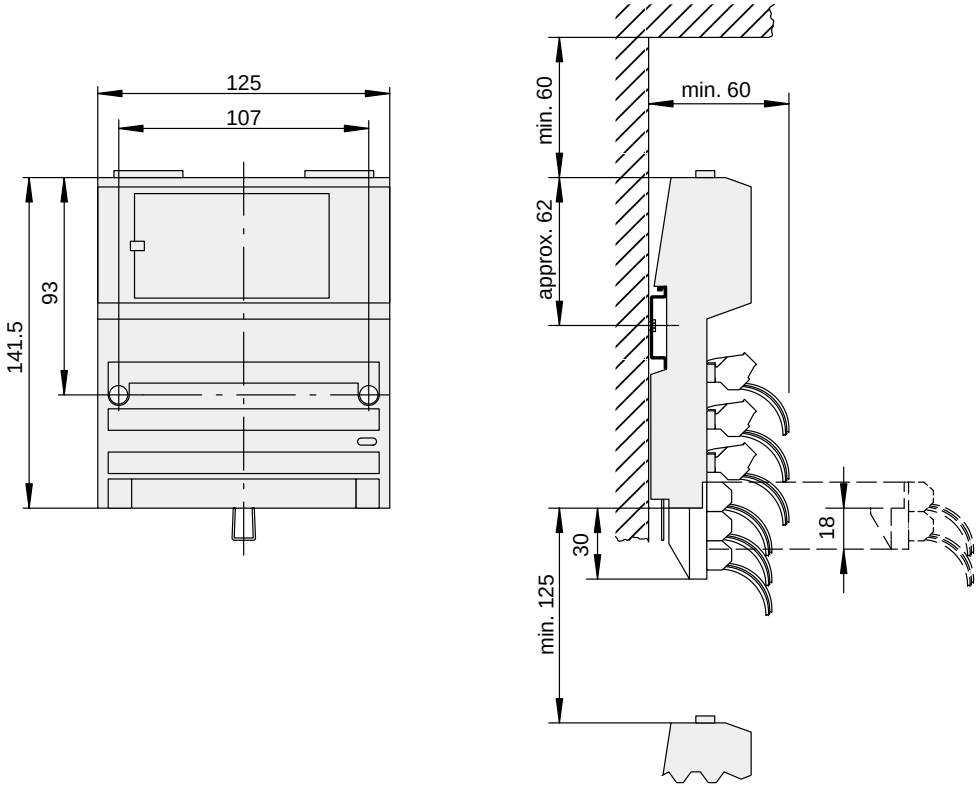


Figure 17 Module dimension drawing

Width: 185 mm
Height: 230 mm

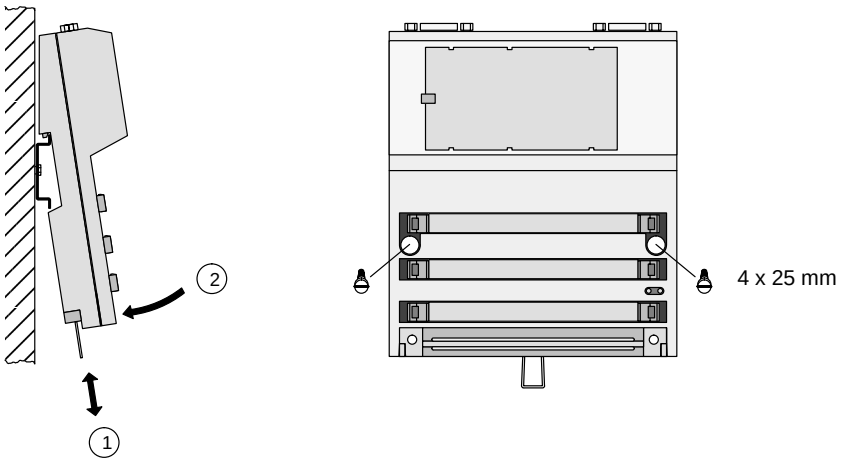


Figure 18 Module installation on a mounting rail (left) and on a wall (right)

2.2 INTERBUS Connection

The INTERBUS requires a 5–conductor cable, available in bulk. Bus cable fabrication is descrbed in the INTERBUS manual. Please pay attention that the pins 5 and 9 of the outgoing remote bus connector must be connected.

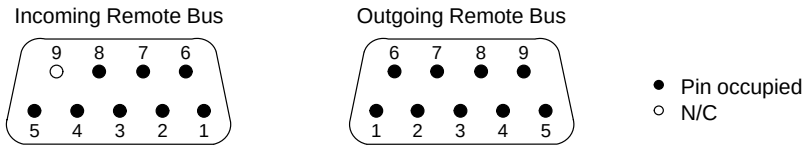


Figure 19 Remote bus port pin assignments

Pin	Incoming Remote Bus	Outgoing Remote Bus	Function
1	DO	DO	Data out
2	DI	DI	Data in
3	GND1	GND	Signal ground
4	GND	GND	Additional fiber optic adapter supply voltage
8	VCC	VCC	
5	VCC1	VCC	Fiber optic adapter supply voltage
6	$\overline{DO}$	$\overline{DO}$	Negated data out
7	$\overline{DI}$	$\overline{DI}$	Negated data in
9	–	RBST	Outgoing plug recognition

2.3 Programming Device Connection

The RS–232C programming device port signals appear on terminals 13 ... 16 of the row 3 terminal strip. Cable 170 NAA 060 00 should be used for the programming device connection.

Terminal	Signal	Function
3.13	D1 (TXD)	Transmitted data
3.14	E2 (GND)	Signal ground
3.15	D2 (RXD)	Received data
3.16		Cable shielding

2.4 Terminal Block Coding and Installation

2.4.1 Terminal Style Selection

The connection of I/O peripherals and the module supply is accomplished through three 18–pole terminal blocks. These are available as a 3–piece set in two variations:

- □ Screw–in terminals, for cable cross sections up to 2.5 mm^2
- □ Spring tension terminals, for cable cross sections up to 1.5 mm^2

Depending upon the specific wiring and the sensor/actuator selection, a 1–, 2–, or 3–row busbar may be required. These are available individually in screw–in and spring tension variants.

2.4.2 Safety Coding

The module may be employed in the safe voltage range (< 42.4 VAC / < 60 VDC). Safety coding prevents that terminal blocks which are wired for the hazardous voltage range can be inadvertently mounted on the module.

Thus the module is delivered with previously coded pin connectors. It lies in the responsibility of the user to code the terminal blocks (not coded at the factory).

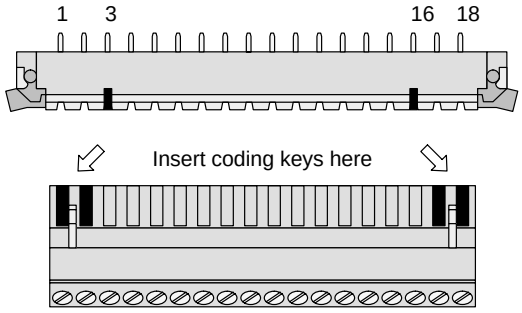


Figure 2 Safety coding demonstrated on the screw–in terminal block

Width: 185 mm
Height: 230 mm

2.4.3 Individual Coding

The user may still undertake an individual coding of the remaining, free coding positions, so as to block–out connectors of the same module types from one another. However, this must not under any circumstances cancel out or alter the safety coding.

2.4.4 Terminal Block Mounting, Removal

To mount terminal blocks, simply press them in pin connectors precoded for 24 VAC (module rows 1 ... 3). To loosen the terminal block press both extractors.

Tightly screw the busbar to the the module’s row 4.

2.5 Input and Output Wiring

The following voltages must be supplied externally (refer to the connection schemes):

- ☐ UB to supply the internal logic (row 1, terminal 18)
- ☐ UB1 to supply the inputs (row 3, terminal 17 or 18)
- ☐ US1 to supply the outputs (row 2, terminal 18)

UB, UB1, and US1 are equipotential to one another, but have potential isolation from the incoming remote bus.

The terminals in busbar rows 4 ... 6 are row–common, but without any connection to the module logic. Different applications will require 1–, 2–, or 3–row busbars.

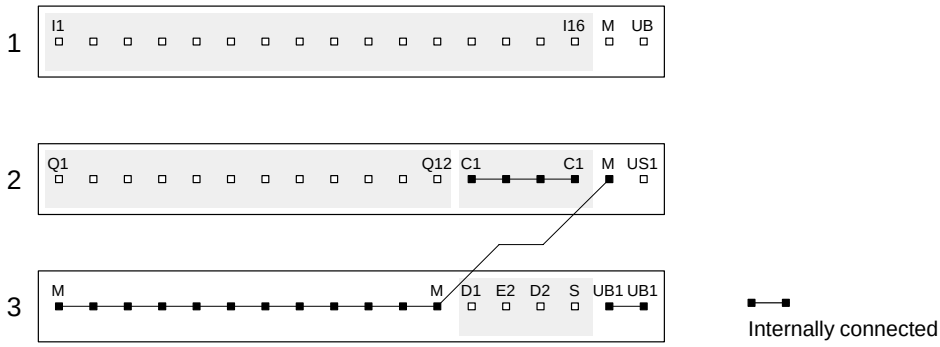


Figure 20 QPR connection mapping

2.5.1 Basic Requirements

The following basic guidelines should be respected:

- ☐ When use is made of an unregulated 24 VDC power supply, the QPR should be protected through the use of an appropriate overvoltage protection (e.g. OVP 001).

- ☐ Utilize shielded cable for sensor connection to the QPR 346 10 in surroundings exhibiting increased interference levels.

- ☐ Outputs of inductive loads require an on–site (parallel to the operating coil) protective circuit with clamping/suppressor diode, when switching components are resident in the output lines, or the lines to the peripherals are very long.

Width: 185 mm
Height: 230 mm

□ Fusing should be dimensioned to match the total current of the connected consumers, but not to exceed 4 A fast–blow for the inputs or 8 A fast–blow for outputs.

2.5.2 Wiring Examples

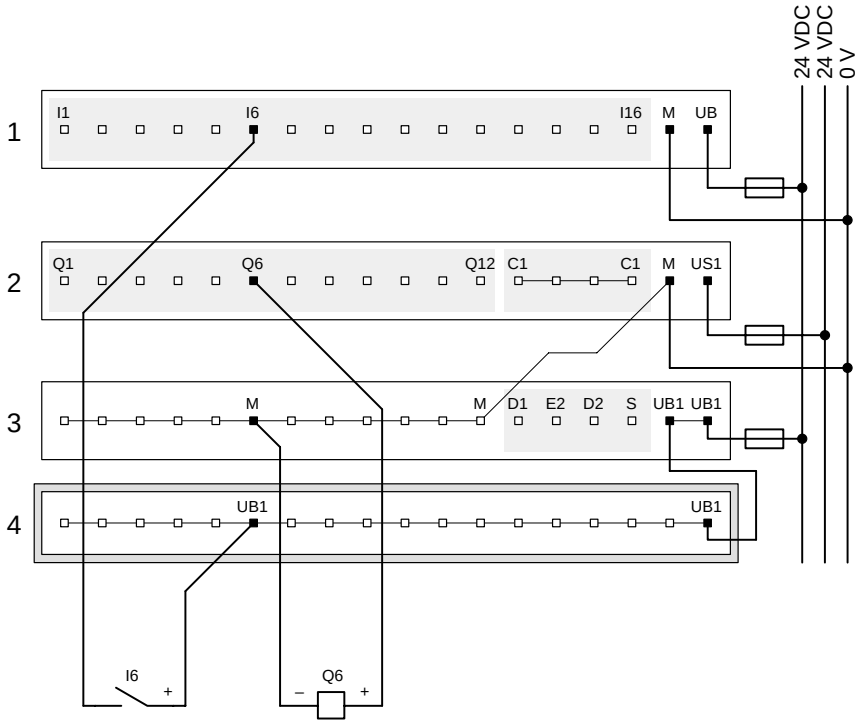


Figure 21 Component selection with 2–wire switching device (push–button/switch) and 2–wire actuator

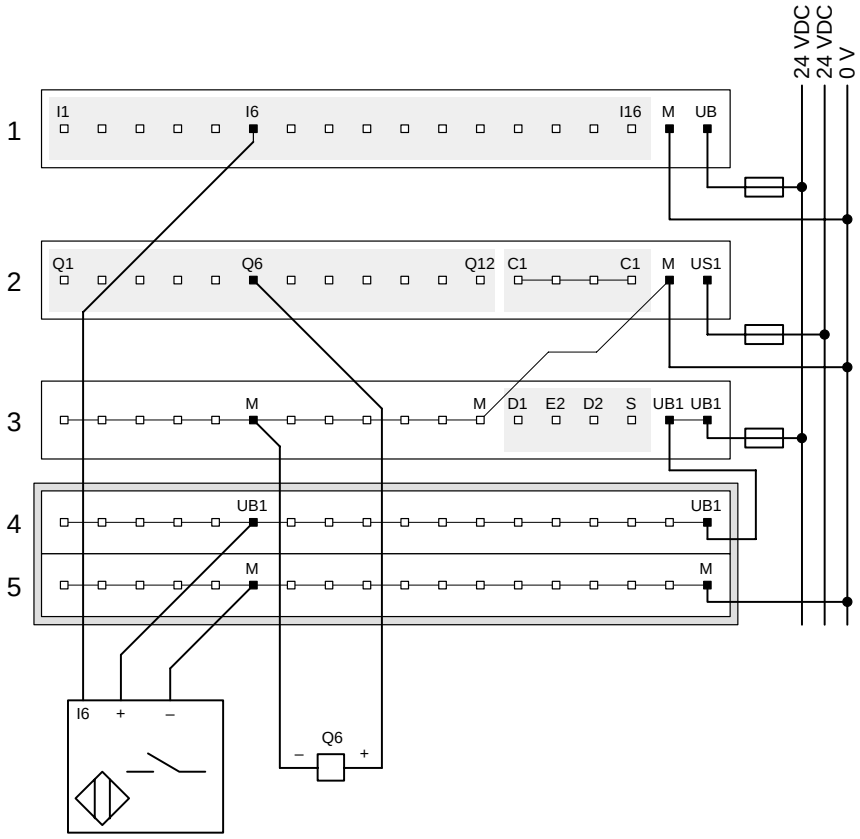


Figure 22 Component selection with 3-wire proximity switch and 2-wire actuator

☞ **Note:** The connection of 4–wire sensors requires the 3–row busbar for PE distribution.

Width: 185 mm
Height: 230 mm

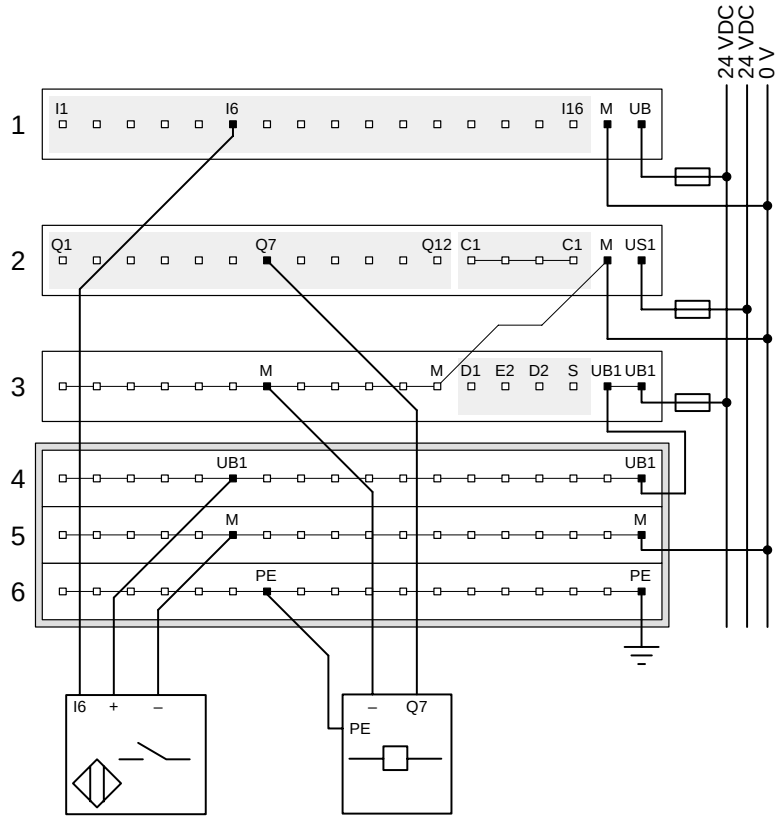


Figure 23 Component selection with 3-wire proximity switch and 3-wire actuator

3 Diagnosis

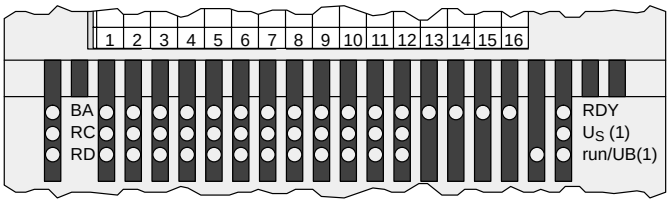


Figure 24 QPR 346 LED status display arrangement

LED	Status	Function
RDY	Green	Ready for service; UB supply voltage for internal logic within tolerance and module not in reset.
	Off	Not ready; UB supply voltage for internal logic not within tolerance or module in reset.
BA	Green	Bus active. Data telegrams are being transferred.
	Off	There is no data telegram transfer.
RC	Red	Remote bus check. The module's incoming bus is connected correctly, and the bus master device is not sending a bus reset signal.
	Off	The incoming bus is not connected correctly, or the bus master device is sending a bus reset signal.
RD	Red	Remote bus disabled. The outgoing remote bus is disabled.
	Off	The outgoing remote bus is enabled.
US1	Green	US1 output voltage is present.
	Off	US1 output voltage is not present. Check the US1 source.
UB1	Green	UB1 input voltage is present.
run	Green	A valid operation list is present and internal logic operations active
	Flashing	An operation list is faulty or not present, or the transfer was disturbed
	Off	A valid operation list is present and internal logic operations halted
1 ... 16 Upper row	Green	Input status (an LED per input); input point active, i.e. input carries "1" signal (logically "ON").
1 ... 12 Middle row	Green	Output status (an LED per output); output point active, i.e. output carries "1" signal (logically "ON").
1 ... 12 Bottom row	Red	Output overload (an LED per output); short circuit or overload on the corresponding output.

Width: 185 mm
Height: 230 mm

4 Technical Specifications

Assignment

Node	INTERBUS
Installation	Mounting rail, or alternatively mounting to a wall or machine housing
Identcode	0233 hex

Module Voltage Supply

Supply voltage	UB = 24 VDC
Current consumption	Typically 70 mA.
Reference potential	M

Process Interface

Inputs	
Sensor supply	UB1 = 24 VDC
Reference potential	M
Complement	16 inputs
Rated signal value	24 VDC
Signal levels	”1” signal +11 ... 30 VDC ”0” signal –3 ... +5 VDC
Input current	6 mA for 24 VDC
Input delay	Typically 0.12 ms for QPR 346 00, QPR 346 20, QPR 346 21 Typically 0.055 ms for QPR 346 10
External fusing	Max. 4 A (fast–blow)
Outputs	
Working voltage	US1 = 24 VDC
Reference potential	M
Complement	12 solid–state outputs
Style	Protected against short circuits and overloads
External fusing	Max. 8 A (fast–blow)
Switched current at max. 60 ^{o}C	Max. 0.5 A per output 6 A per module
Resistive load	12 W per output
Inductive load	12 W per output
Bulb load	1.2 W per output
Switching cycle	Inductive load (0.5 A) 1000/h resistive load (0.5 A) 100/s bulb load (1.2 W) 8/s

Potential Relationships

Equipotential	UB, UB1, US1 to another
Potential isolation	UB, UB1, US1 to the arriving remote bus

INTERBUS Data Interface

Port mapping	Refer to page 52
Transmission rate	500 Kbps
Permissable line lengths	Refer to system data

Fault evaluation

LED status display	Remote bus functions, status, ... (refer to section 3)
Fault message	Module fault to the bus master

Mechanical Design

Module	In standard housing
Dimensions (W x H x D)	125 x 142 x 44 mm
Weight	260 g

Remote Bus Connection Styles

Incoming remote bus	Sub–D9 plug
Outgoing remote bus	Sub–D9 socket

Process Connection Styles

Rows 1 ... 3	Plugable terminal blocks with screw–in or spring tension terminals
Row 4	Threaded busbar with screw–in or spring tension terminals

Environmental Conditions

Regulations	Meets VDE 0160, UL 508
Safety classification	IP20
Ventilation	Module hanging, natural convection
Ambient temperature	0...60°C
Power dissipation	Typically 4 W

Width: 185 mm
Height: 230 mm

62 170 QPR 346 00, ... 170 QPR 346 21

Appendix B
Configuration Forms

DIN A4 coding forms are available for the individual network types. Their use should simplify the generation, and most especially the coding, of networks. These forms are obtainable as form pad blocks (type 870 USE 001 02). The block contains

- 70 logic operation network
- forms
- 10 up–counter
- forms
- 10 up/down–counter
- forms
- 10 on–delay forms

These forms are also especially suitable as copy masters. They are depicted on the following pages in reduced size.

Width: 185 mm
Height: 230 mm

Logic Operation Network

Plant: _____

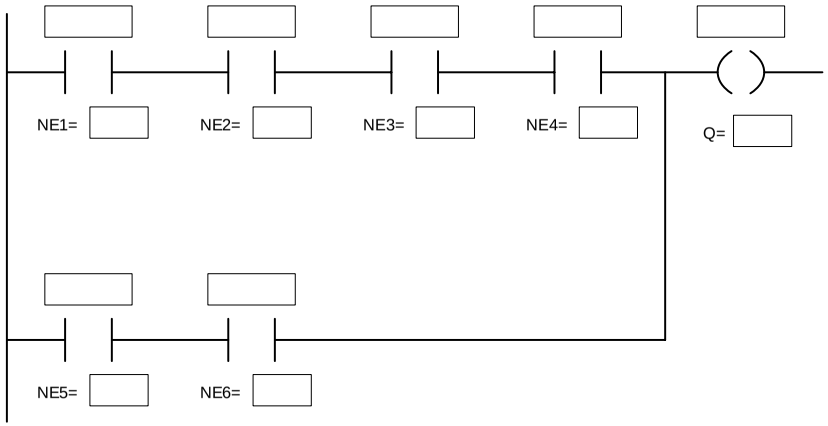
Station: _____

Program: PI

Network: N

Author: _____

Date: _____



Network Elements (NE)			
Operand	Bit	Value	Inversion
Q	[1 ... o]	+ 0	+ 128
BM →	[1 ... 16]	+ 16	
I	[1 ... i]	+ 32	
I ↑	[1 ... i]	+ 48	
→ BM	[1 ... 16]	+ 64	
M	[1 ... 16]	+ 80	
M ↑	[1 ... 16]	+ 96	
C	[1 ... 8]	+ 112	
T	[1 ... 7]	+ 120	
K0 (0 const.)	0		
$\overline{K0}$ (1 const.)	128		

o, i = max. operand address allowed (= QPR output/input complement)

Examples					
	Operand	Address	Offset	Inversion	NE =
$\overline{Q7}$ inverted	$\overline{Q7}$	7	0	128	135
Input 5 with positive edge detection	I5↑	5	48	–	53
Bit 3 from bus master	BM3→	3	16	–	19

Up–Counter

Plant: _____

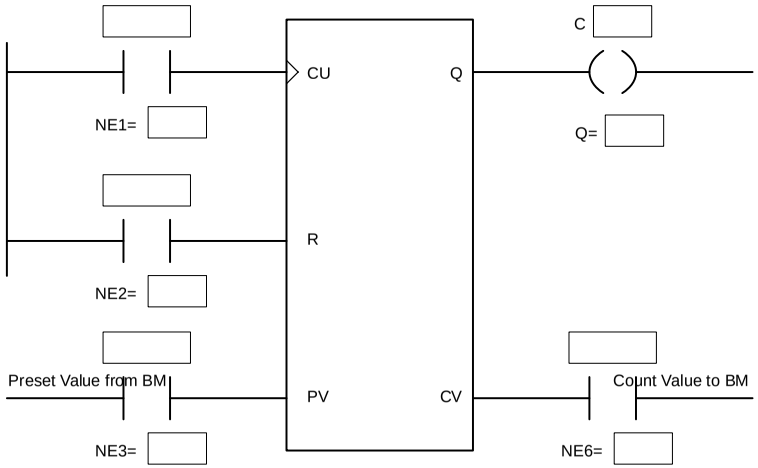
Station: _____

Program: PI

Network: N

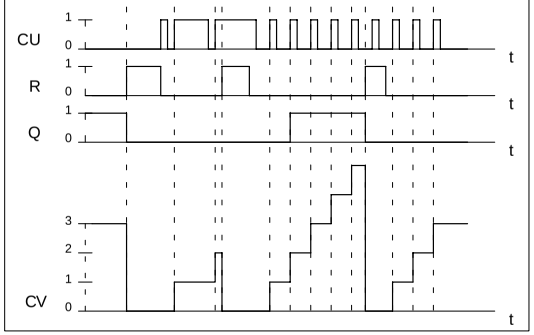
Author: _____

Date: _____



PV initialization value = 256 x NE5 (0 – 255) + NE4 (0 – 255)

Action Chart



Network Elements (NE)

Operand	Bit	Value	Inversion
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BM →	[1 ... 16]	+ 16	
I	[1 ... i]	+ 32	
I ↑	[1 ... i]	+ 48	
→ BM	[1 ... 16]	+ 64	
M	[1 ... 16]	+ 80	
M↑	[1 ... 16]	+ 96	
C	[1 ... c]	+ 112	
T	[1 ... 7]	+ 120	
K0 (0 const.)	0		
$\overline{K0}$ (1 const.)	128		

o, i, c = max. operand address allowed (= QPR output/input/up–counter network complement)

Examples

	Operand	Address	Offset	Inversion	NE =
$\overline{Q7}$ inverted	$\overline{Q7}$	7	0	128	135
Input 5 with positive edge detection	I5↑	5	48	–	53
Bit 3 from bus master	BM3→	3	16	–	19

Up/Down–Counter

Plant: _____

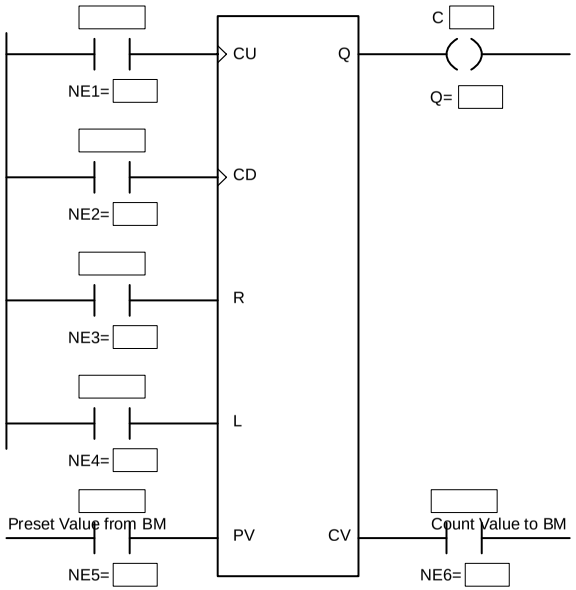
Station: _____

Program: PI

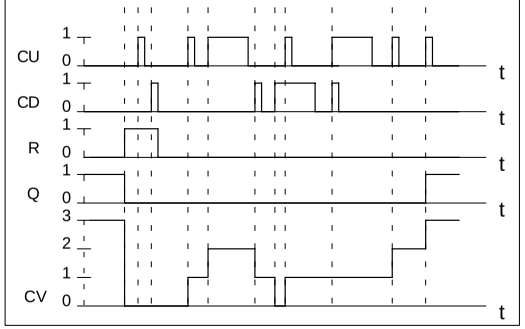
Network: N

Author: _____

Date: _____



Action Chart



Network Elements (NE)

Operand	Bit	Value	Inversion
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BM →	[1 ... 16]	+ 16	
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→ BM	[1 ... 16]	+ 64	
M	[1 ... 16]	+ 80	
M↑	[1 ... 16]	+ 96	
C	[5 ... 8]	+ 112	
T	[1 ... 7]	+ 120	
K0 (0 const.)	0		
$\overline{K0}$ (1 const.)	128		

o, i = max. operand address allowed (= QPR output/input complement)

Examples

	Operand	Address	Offset	Inversion	NE =
$\overline{Q7}$ inverted	$\overline{Q7}$	7	0	128	135
Input 5 with positive edge detection	I5↑	5	48	–	53
Bit 3 from bus master	BM3→	3	16	–	19

On–Delay

Network Elements (NE)

Operand	Bit	Value	Inversion
Q	[1 ... o]	+ 0	+ 128
BM →	[1 ... 16]	+ 16	
I	[1 ... i]	+ 32	
I ↑	[1 ... i]	+ 48	
→ BM	[1 ... 16]	+ 64	
M	[1 ... 16]	+ 80	
M ↑	[1 ... 16]	+ 96	
C	[1 ... 8]	+ 112	
T	[1 ... 7]	+ 120	
K0 (0 const.)	0		
$\overline{K0}$ (1 const.)	128		

o, i = max. operand address allowed (= QPR output/input complement)

Examples

	Operand	Address	Offset	Inversion	NE =
$\overline{Q7}$ inverted	$\overline{Q7}$	7	0	128	135
Input 5 with positive edge detection	I5↑	5	48	–	53
Bit 3 from bus master	BM3→	3	16	–	19

On–Delay

Plant: _____

Station: _____

Program: PI

Network: N

Author: _____

Date: _____

Width: 185 mm
Height: 230 mm

68 Configuration Forms

Index

Breite: 185 mm
Höhe: 230 mm

70 Index