EXTENDED MEMORY

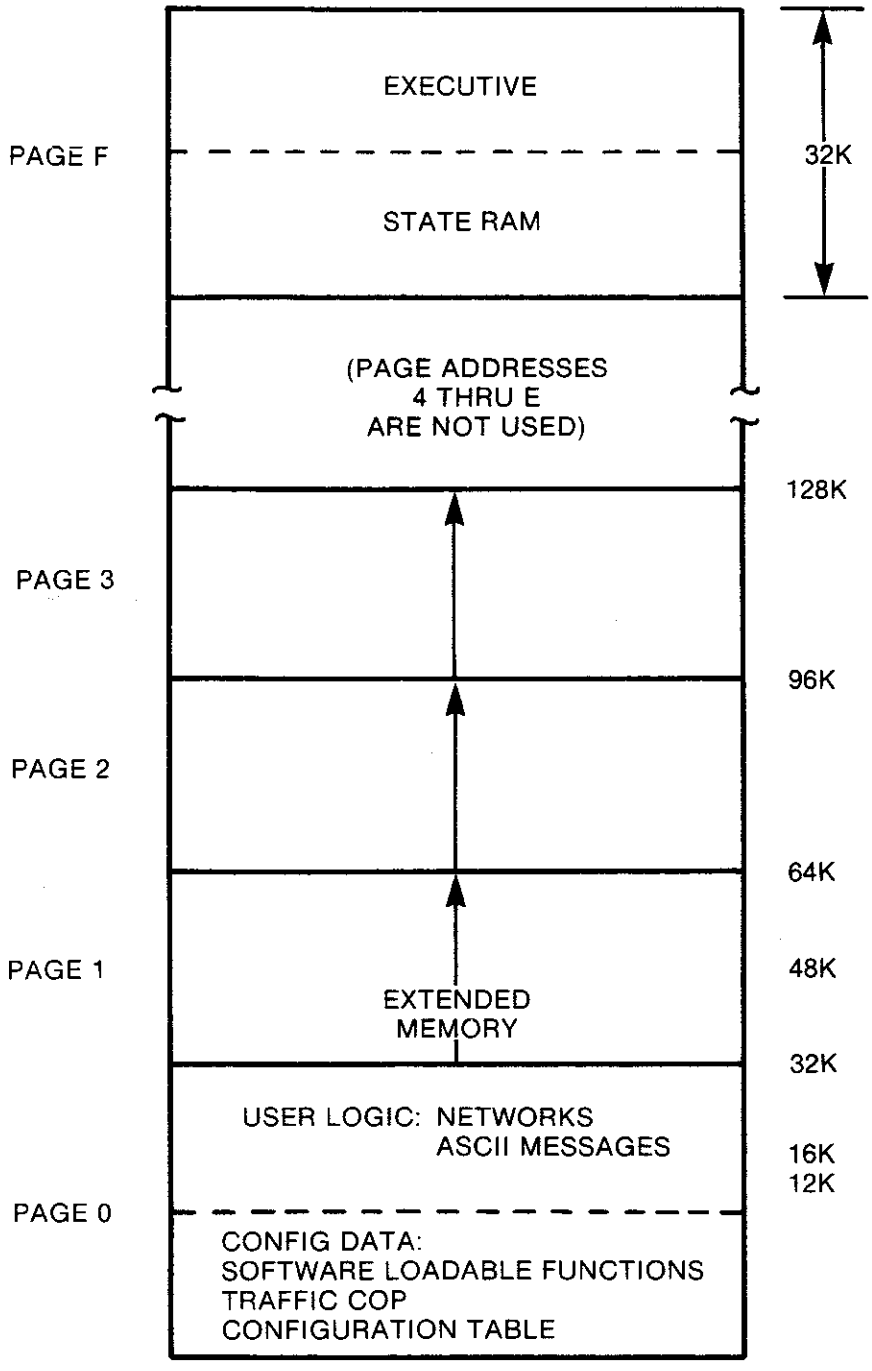
The 584L Controller product line has been expanded to include 4 new memory sizes: 48 K, 64 K, 96 K and 128 K. The increased memory capacity, termed "Extended Memory," over the existing 32 K memory, will provide mass storage capacity for data that can be stored in BCD, 16 bit binary, hexadecimal, or ASCII format.

The Extended Memory will store data in a group of files made up of storage registers using a 6XXXX reference number. Up to 10 data files are available, with each file having up to 10,000 registers numbered 60000 to 69999. Memory size of the 584L over 32 K will determine the quantity of storage registers available at the rate of 1 storage register for each word of extended memory. As an example, a 48 K 584L Controller will translate into approximately 16384 storage registers. The first file will have the first 10,000 registers numbered 60000 to 69999 and the second file will have the remaining 6,384 storage registers, numbered 60000 to 66383.

584L EXTENDED MEMORY FILE STRUCTURE

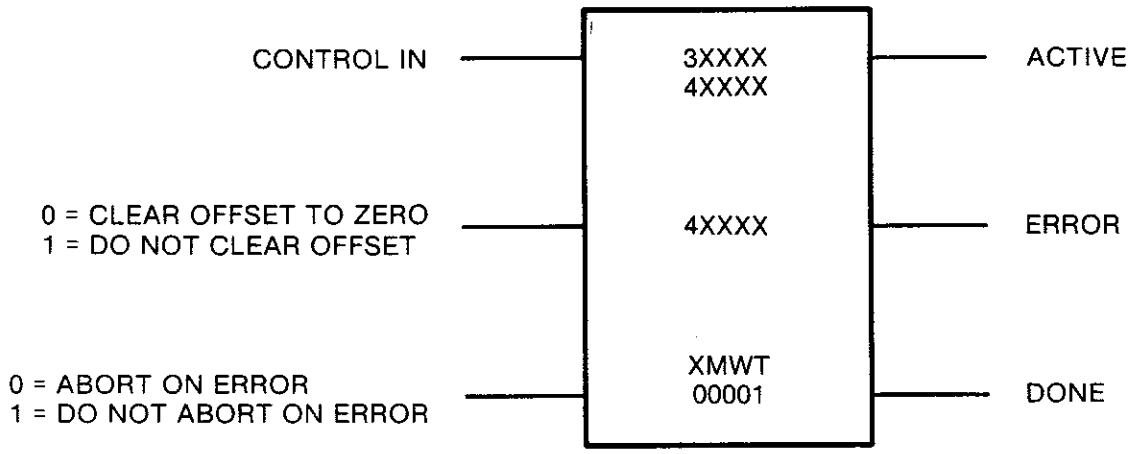
	File 1	File 2	Up To	File 10
Registers	60000 60001 60002	60000 60001 60002		60000 60001 60002
	69999	69999		69999

584L EXTENDED MEMORY MAP CONFIGURATION



EXTENDED MEMORY WRITE

This function block copies a table of holding (4XXXX) or input (30XXX) registers to a table of 6XXXX registers located within the extended memory area of a 584L.



Function Block

The top node is the source table and can be either:

the first 30XXX reference number in a table of input registers or
the first 4XXXX reference number in a table of holding registers

The middle node must be a holding register (4XXXX). This register is the first in a table of 6 holding registers, which are allocated as follows.

1. 4XXXX = status word
2. 4XXXX + 1 = extended memory file number (1 - 10)
3. 4XXXX + 2 = first 6XXXX register in destination table (0 to 9999)
4. 4XXXX + 3 = number of registers to be transferred per scan (0 to 9999)
5. 4XXXX + 4 = number of registers transferred thus far. Termed "offset"
6. 4XXXX + 5 = total number of registers to be transferred

The bottom node contains the symbol XMWT, and the value 00001 is automatically displayed when the block is programmed.

Inputs

Top: Control in. Every scan this node is powered, the data transfer will occur.

Middle: When powered, the offset value will not be cleared. When not powered, the offset value will be cleared to zero before the instruction is solved.

Bottom: When powered, the 584L will not automatically power down when a parity diagnostic error is detected.

Outputs

Top: Active. Passes power from the time the top input is initially asserted, until the specified number of registers have been transferred.

Middle: Error. Passes power if the top input is powered and an error is detected.

Bottom: Done. Passes power for one scan when all registers have been transferred.

EXTENDED MEMORY WRITE

Middle Node Register Usage

The middle node defines a table of 6 holding (4XXXX) registers as follows: 4XXXX = Status Word (see details page 17-9)

Bit #	Definition
0	File parameter error
1	SA parameter error
2	Count parameter error
3	Offset parameter error
4	Max parameter error
5	
6	Non-existent SRAM
7	
8	
9	Offset parameter too large on entry
10	File boundary crossed
11	Done
12	Busy
13	Non-existent x-mem
14	X-mem parity error
15	Power up diagnostic error

4XXXX + 1 = File Number

The extended memory area is divided into 10 files. Each file has 10,000 registers. This register specifies which file (1-10) is to be used.

4XXXX + 2 = Start Address

Specifies the starting address (0 to 9999) in the file specified by the previous register. 0 = first register, 9999 = 10,000th register.

4XXXX + 3 = Number of Registers to be Transferred per Scan

This register specifies the number of registers to be transferred per scan. Range = 0 to 9999. 0 = 1 register, 9999 = 10,000 registers.

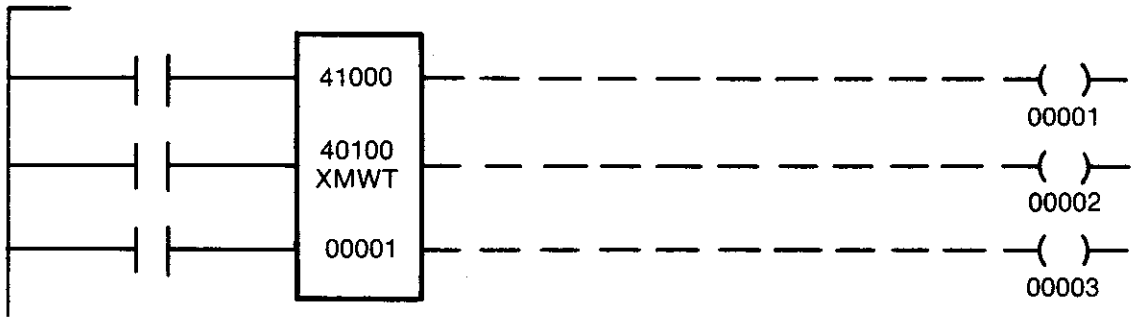
4XXXX + 4 = Offset

This is the running total of the number of registers which have been transferred thus far.

4XXXX + 5 = Total Number of Registers to be Transferred.

This register specifies the maximum number of registers to be transferred when the block is powered. Range = 0 to 9999.

EXTENDED MEMORY WRITE EXAMPLE



In this example, a block of 1000 4XXXX registers is written in one scan to extended memory. The block starts at register 41000 and is written to a block starting at register 2000 in file two.

The control table, displayed in the following figure, begins at register 40100. The value in register 40101, 0002, is the extended memory file number. The value 2000 in register 40102 is the location in extended memory that the block of registers is written to. The value 1000 in register 40103 is the number of registers transferred per scan. Register 40104 contains the offset count which changes throughout the function. The value 1000 in register 40105 is the total number of registers being transferred.

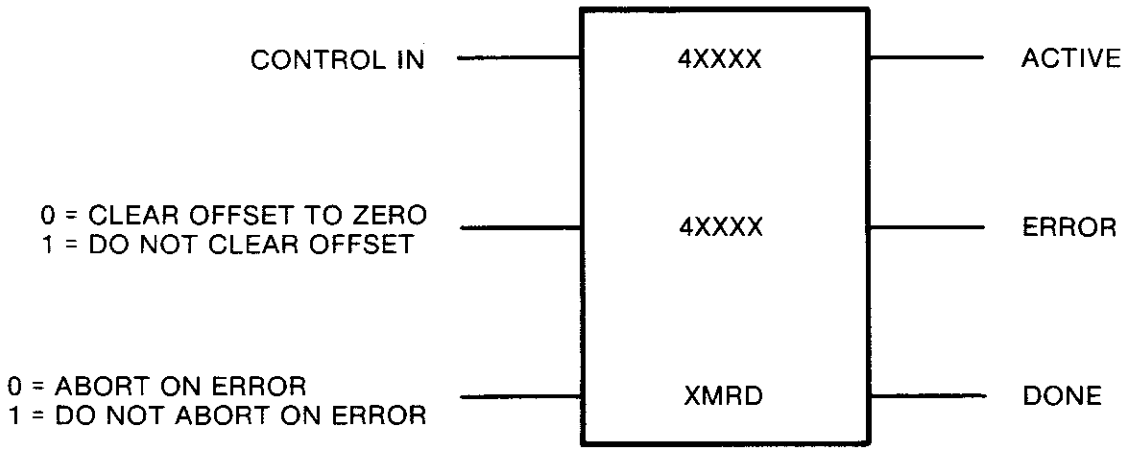
CONTROL TABLE

40100 Status Word	
40101	0002
40102	2000
40103	1000
40104	0000
40105	1000

Coil 00001 is energized when the function block is active and coil 00003 is energized when the write is complete. Coil 00002 is used to indicate an error.

EXTENDED MEMORY READ

This function block copies a table of extended memory registers (6XXXX) in a 584L to a table of holding registers (4XXXX).



Function Block

The top node must be a holding register (4XXXX). This register is the first in a table of 6 holding registers, which are allocated as follows.

1. 4XXXX = status word
2. 4XXXX + 1 = file number (1 - 10)
3. 4XXXX + 2 = first 6XXXX register in destination table (60000 - 69999)
4. 4XXXX + 3 = number of registers to be transferred per scan
5. 4XXXX + 4 = number of registers transferred. Termed "offset"
6. 4XXXX + 5 = maximum number of registers to be transferred

The middle node is the destination table and must be the first 4XXXX reference number in a table of holding registers which will receive the data transferred from the extended memory storage registers (6XXXX).

The bottom node contains the symbol XMRD, and the value 00001 is automatically displayed when the block is programmed.

Inputs

Top: Control in. Every scan this node is powered, the data transfer will occur.

Middle: When powered, the offset value will not be cleared. When not powered, the offset value will be cleared to zero before the instruction is solved.

Bottom: When powered, the 584L will not automatically power down when a parity diagnostic error is detected.

Outputs

Top: Active. Passes power from the time the top input is initially asserted, until the specified number of registers have been transferred.

Middle: Error. Passes power if the top input is powered and an error is detected.

Bottom: Done. Passes power for one scan when all registers have been transferred.

EXTENDED MEMORY READ

Top Node Register Usage

The top node defines a table of 6 holding (4XXXX) registers as follows: 4XXXX = Status Word (See details page 17-9)

Bit #	Definition
0	File parameter error
1	SA parameter error
2	Count parameter error
3	Offset parameter error
4	Max parameter error
5	
6	Non-existent SRAM
7	
8	
9	Offset parameter too large on entry
10	File boundary crossed
11	Done
12	Busy
13	Non-existent x-mem
14	X-mem parity error
15	Power up diagnostic error

4XXXX + 1 = File Number

The extended memory area is divided into 10 files. Each file has 10,000 registers. This register specifies which file (1-10) is to be used.

4XXXX + 2 = Start Address

Specifies the starting address (0 to 9999) in the file specified by the previous register. 0 = first register, 9999 = 10,000th register.

4XXXX + 3 = Number of Registers to be Transferred per Scan

This register specifies the number of registers to be transferred per scan. Range = 0 to 9999. 0 = 1 register, 9999 = 10,000 registers.

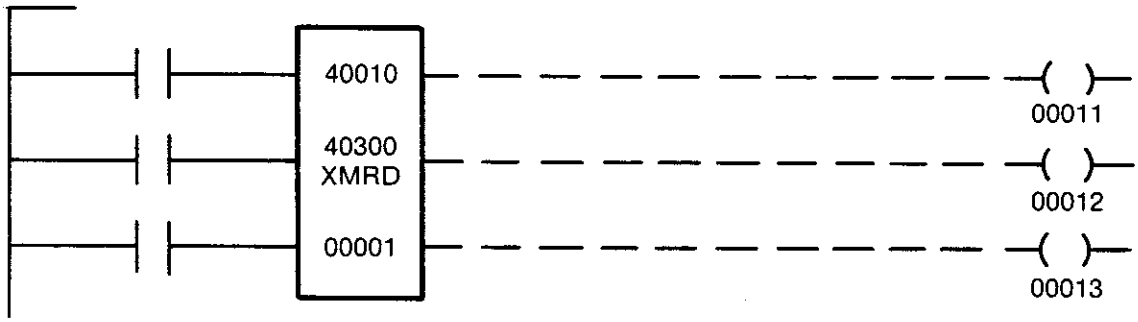
4XXXX + 4 = Offset

This is the running total of the number of registers which have been transferred thus far.

4XXXX + 5 = Total Number of Registers to be Transferred.

This register specifies the maximum number of registers to be transferred when the block is powered. Range = 0 to 9999.

EXTENDED MEMORY READ EXAMPLE



In this example, a block of 1400 6XXXX registers are read in two scans (700 per scan) from extended memory. The block starts at register 3000 in file three and is written to a block starting at register 40300.

The control table, displayed in the following figure, begins at register 40010. The value in 40011, 0003, is the extended memory file number. The value 3000 in register 40012 is the starting register in the extended memory block that is read. The value 0700 in register 40013 is the number of registers transferred per scan. Register 40014 contains the offset count which changes throughout the function. The value in register 40015, 1400, is the total number of registers being transferred.

CONTROL TABLE

40010 Status Word	
40011	0003
40012	3000
40013	0700
40014	0000
40015	1400

Coil 00011 is energized when the function block is active and coil 00013 is energized when the read is complete. Coil 00012 is used to indicate an error.

EXTENDED MEMORY STATUS WORD FORMAT

Bit 0 — File Parameter Error

The second register in the control block (4XXXX + 1) contains an illegal value for the number of files. Legal values range from 1 to 10.

Bit 1 — Starting Address Parameter Error

The third register in the control block (4XXXX + 2) contains an illegal value for the starting address. Legal values range from 0 to 9999 except in the last file. The legal values for the last file number and its last address are:

584L Size	XMEM Size	Last File	Last Address
48K	16K	2	6383
64K	32K	4	2767
96K	64K	7	5535
128K	96K	10	8403

Bit 2 — Count Parameter Error

The fourth register in the control block (4XXXX + 3) contains an illegal value. Valid count values range from 0 to 9999.

Bit 3 — Offset Parameter Error

The fifth register in the control block (4XXXX + 4) contains an illegal value. Valid offset values range from 0 to 9999.

Bit 4 — Maximum Register Parameter Error

The sixth register in the control block (4XXXX + 5) contains an illegal value. Valid maximum register values range from 0 to 9999.

Bit 5 — Not Used.

Bit 6 — Non-existent State RAM

This bit is set when the 4XXXX or 3XXXX register, specified in the node as source or destination, plus the maximum number of registers to transfer will exceed the last 3XXXX or 4XXXX register available in the 584 machine configuration. The bit is set the first time the node is active even in the multiple scan mode. This bit is set even if the actual transfer that would cause the error occurs in the latter scan. No data is transferred as long as the condition exists.

Bit 7 — Not Used.

Bit 8 — Not Used.

Bit 9 — Offset Parameter Too Large On Entry

If you are in the do-not-clear-offset mode upon entering the node and the offset value is equal to or greater than the maximum number of registers to be transferred, this bit is set. No data transfer is performed.

Bit 10 — File Boundary Crossed

This bit is set during the scan that results in data being transferred to or from extended memory and the address crosses a file boundary. On single scan transfers it is set for the scan that the node is active and the file crossing occurs. During multiple scan transfers the bit is set during the scan that the transfer occurs and remains on for all transfers to the upper file. The file number in the control block is not changed.

Bit 11 — Done

This bit is set when a transfer is complete even if a parity error was detected during the transfer.

Bit 12 — Busy

This bit is set on multiple scan transfers, when the scan the node is active and the transfer is not complete. The busy bit is not set if all validation checks have not been successful.

Bit 13 — Non-existent XMEM

This bit is set if the read/write data transfer will reference a register address that does not exist in the current configuration. On a single scan transfer, if the sum of the starting address and the count references a register address that does not exist in the current configuration, the bit is set. On multiple scan transfers, if the sum of the starting address and the maximum number of registers to be transferred references a value outside the configuration, the bit is set. The setting of the bit inhibits data transfer even if the transfer to or from the non-existent registers will not occur during the current scan.

Bit 14 — XMEM Parity Error

This bit is set when the logic detects a parity error when attempting to read an extended memory location.

Bit 15 — Power-up Diagnostic Failure

This bit is set when the node is active and an error was previously detected during the extended memory power-up diagnostic.