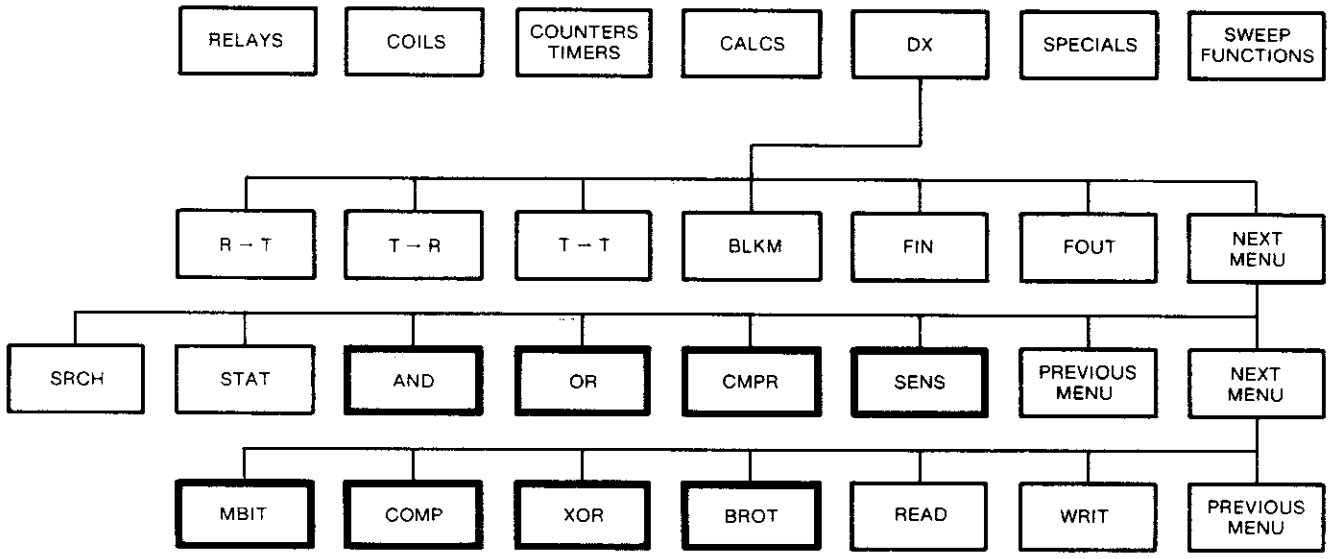
DATA TRANSFER (DX) MATRIX FUNCTIONS



DATA TRANSFER (DX) MATRIX FUNCTIONS

Matrix

A matrix is a sequence of data bits formed by consecutive 16 bit words derived from tables. The figure below depicts the bit matrix derived from 3 consecutive holding registers. Note the bit numbering scheme.

Holding Register Table		Bit Matrix															
40001	=	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
40002	=	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
40003	=	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48

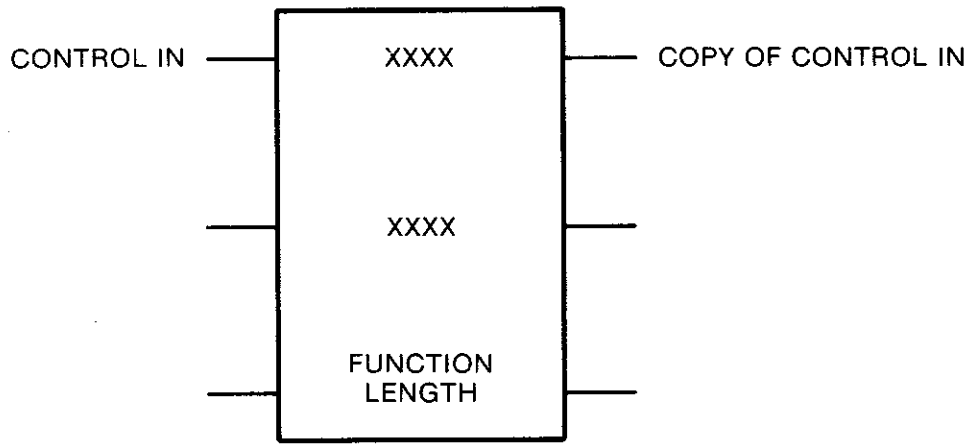
The plural form of matrix is "matrices".

DX Matrix Functions

Data transfer or "DX" matrix functions operate on the bit pattern within a table. These functions are available under the DX portion of the programming menu and include:

- Logical "And" of two matrices (AND)
- Logical "Or" of two matrices (OR)
- Logical "Exclusive Or" of two matrices (XOR)
- Logical "complement" of one matrix (COMP)
- Logical compare of two matrices (CMPR)
- Bit sense (SENS)
- Bit modify (MBIT)
- Bit rotate (BROT)

Format



The figure above illustrates the general format of a data transfer matrix function block. The block consumes 1 horizontal and 3 vertical nodes. The bottom node within the block specifies the function and the matrix length in 16 bit words.

The top input is always the "control in" input and the top output is always a copy of the "control in" input. This allows DX blocks to be cascaded.

The top and middle nodes within the block, and all other inputs and outputs vary with each function.

DATA TRANSFER (DX) MATRIX FUNCTIONS

Length

Minimum table length is one (one 16 bit word or register). Maximum table length is dependent on the DX function and on the controller type (16 or 24 bit CPU). See figure below.

Controller Model	AND	OR	XOR	COMP	CMPR	MBIT	SENS	BROT
*584A Level 1&2	100	100	100	100	100	255	255	100
*584M Level 1&2	100	100	100	100	100	255	255	100
*584L Level 1	100	100	100	100	100	255	255	100
**584A Level 3	100	100	100	100	100	600	600	100
**584L Level 2	100	100	100	100	100	600	600	100

* = Bit CPU
** = 24 Bit CPU

Pointer

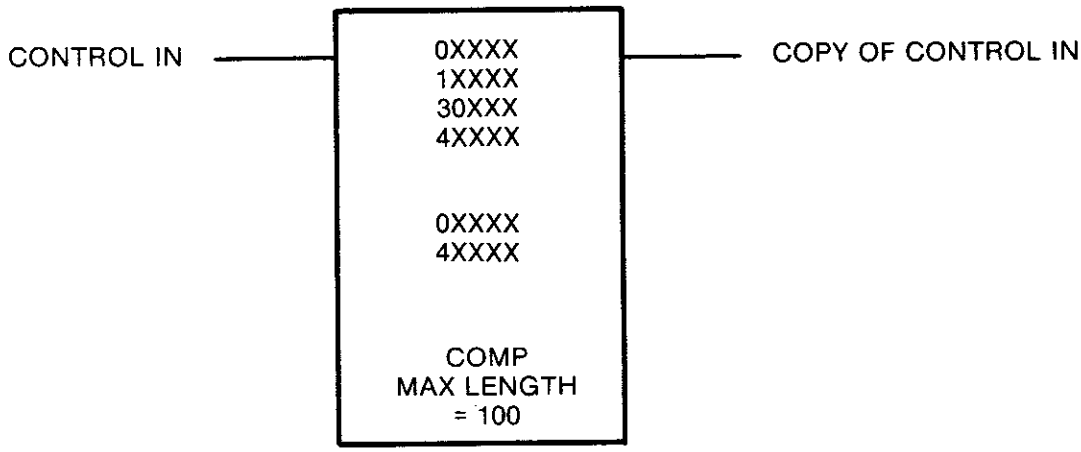
The compare, bit modify, and bit sense functions utilize a pointer to indicate which bit in the matrix is being operated on. A register used to hold the pointer value for the bit modify or bit sense function may be manipulated by other logic functions (timers, counters, arithmetic operations, etc.).

Discrete Tables

Discrete references are used in groups of 16. The reference number used is the first in the group; the other 15 references are implied. Additionally, only reference numbers which appear in the "first of 16" table shown on page 12-12 may be used, e.g. 1, 17, 33 etc.

COMPLEMENT

This function copies the complemented or inverted bit pattern (all "1's" are replaced by "0's, all "0's" are replaced by "1's") of one matrix into a second matrix.



Function Block

The top node is the data source and can be one of the following:

- the first 0XXXX reference number in a table of output references
- the first 1XXXX reference number in a table of input references
- the first 30XXX reference number in a table of input registers
- the first 4XXXX reference number in a table of holding registers.

The middle node is the destination and can be one the following:

- the first 0XXXX reference number in a table of output references
- the first 4XXXX reference number in a table of holding registers.

The bottom node contains the symbol COMP and number specifying table length. Maximum table length = 100 (maximum number of bits in matrix = 1600)

Inputs

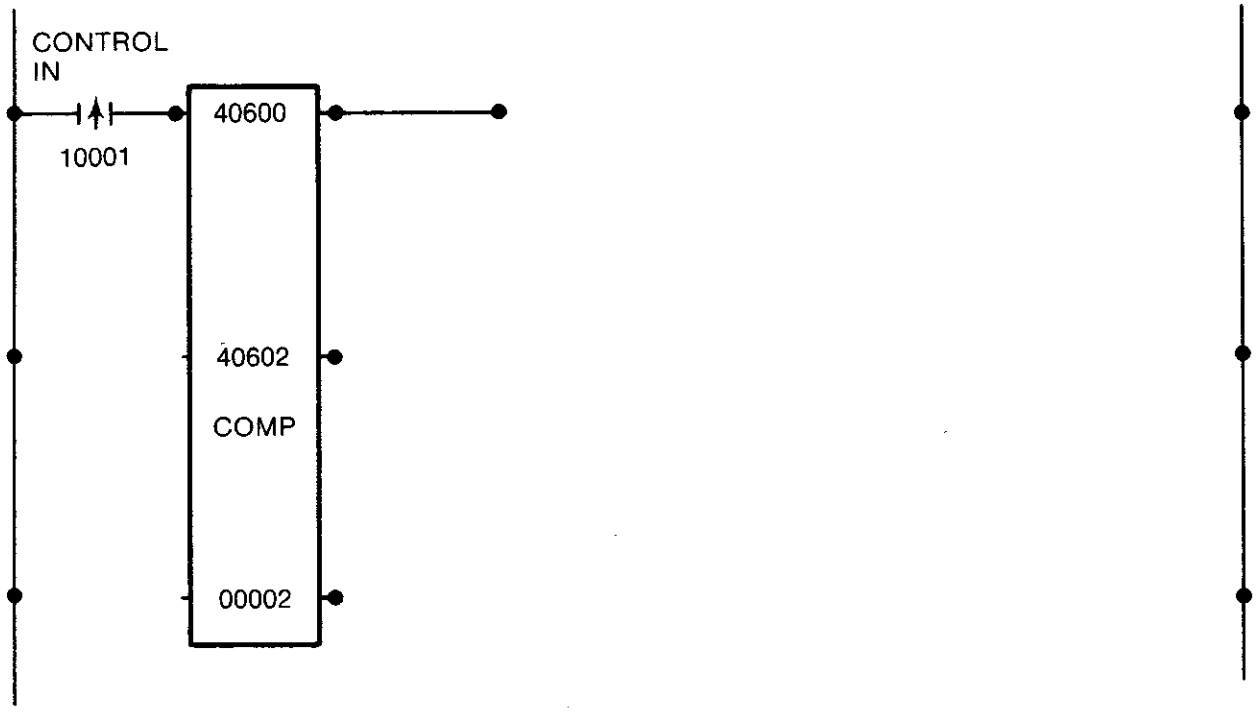
Top: Control in. Every scan this node is powered, the complement function is performed. A transitional contact should be used if single operations are desired.

Outputs

Top: Passes power when top input is powered.

COMPLEMENT BLOCK

Network #53



SOURCE MATRIX

40600 = 1111111100000000	40601 = 1111111100000000

DESTINATION MATRIX BEFORE MOVE

40602 = 1111111111111111	40603 = 0000000000000000

DESTINATION MATRIX AFTER MOVE

40602 = 0000000011111111	40603 = 0000000011111111

Network Description

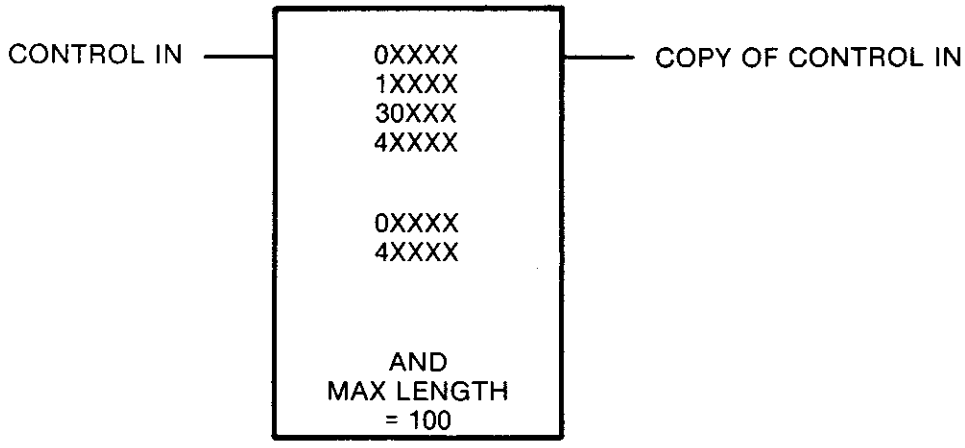
Whenever 10001 passes power, the complement of the bit matrix formed by registers 40600 and 40601 will be copied into a second matrix formed by registers 40602 and 40603.

WARNING: The destination for this function can be a group of outputs. This function will override any disabled coils within this group without enabling them.

AND

This function logically "ands" each bit in a source matrix with its corresponding bit in a second (destination) matrix. If both bits are a "1", the bit in the destination matrix will be set to a "1". If either or both bits are a "0", the bit in the destination matrix will be cleared to a "0". A truth table follows:

Bit 1 Source	Bit 1 Destination Before Move	Bit 1 Destination After Move
0	0	0
0	1	0
1	0	0
1	1	1



Function Block

The top node is the data source and can be one of the following:

- the first 0XXXX reference number in a table of output references
- the first 1XXXX reference number in a table of input references
- the first 30XXX reference number in a table of input registers
- the first 4XXXX reference number in a table of holding registers.

The middle node is the destination and can be one of the following:

- the first 0XXXX reference number in a table of output references
- the first 4XXXX reference number in a table of holding registers.

The bottom node contains the symbol and a number specifying table length. Maximum table length = 100 (maximum number of bits in matrix = 1600)

Inputs

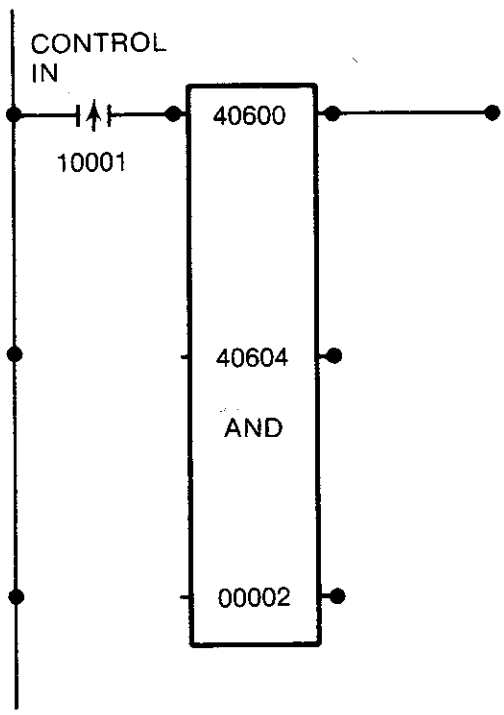
Top: Control in. Every scan this node is powered, the AND function is performed. A transicontact should be used if single operations are desired.

Outputs

Top: Passes power when top input is powered.

AND

Network #54



SOURCE MATRIX

40600 = 1111111100000000	40601 = 1111111100000000

DESTINATION MATRIX BEFORE MOVE

40604 = 1111111111111111	40605 = 0000000000000000

DESTINATION MATRIX AFTER MOVE

40604 = 1111111100000000	40605 = 0000000000000000

Network Description

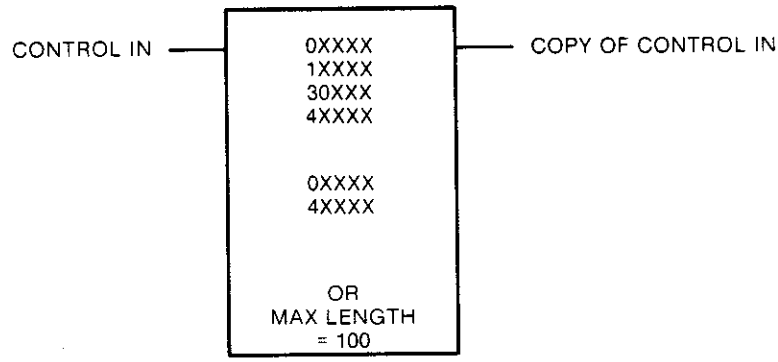
Whenever 10001 passes power, the bit matrix formed by registers 40600 and 40601 will be ANDed with the bit matrix formed by registers 40604 and 40605. The result of this operation will be copied into registers 40604 and 40605.

WARNING: The destination for this function can be a group of outputs. This function will override any disabled coils within this group without enabling them.

OR

This function logically "ors" each bit in a source matrix with its corresponding bit in a second (destination) matrix. If either or both bits is a "1", the bit in the destination matrix will be set to a "1". If both bits are a "0", the bit in the destination matrix will be cleared to a "0". A truth table follows:

Bit 1 Source	Bit 1 Destination Before Move	Bit 1 Destination After Move
0	0	0
0	1	1
1	0	1
1	1	1



Function Block

The top node is the data source and can be one of the following:

- the first 0XXXX reference number in a table of output references
- the first 1XXXX reference number in a table of input references
- the first 30XXX reference number in a table of input registers
- the first 4XXXX reference number in a table of holding registers.

The middle node is the destination and can be one of the following:

- the first 0XXXX reference number in a table of output references
- the first 4XXXX reference number in a table of holding registers.

The bottom node contains the symbol OR and a number specifying table length. Maximum table length = 100 (maximum number of bits in matrix = 1600)

Inputs

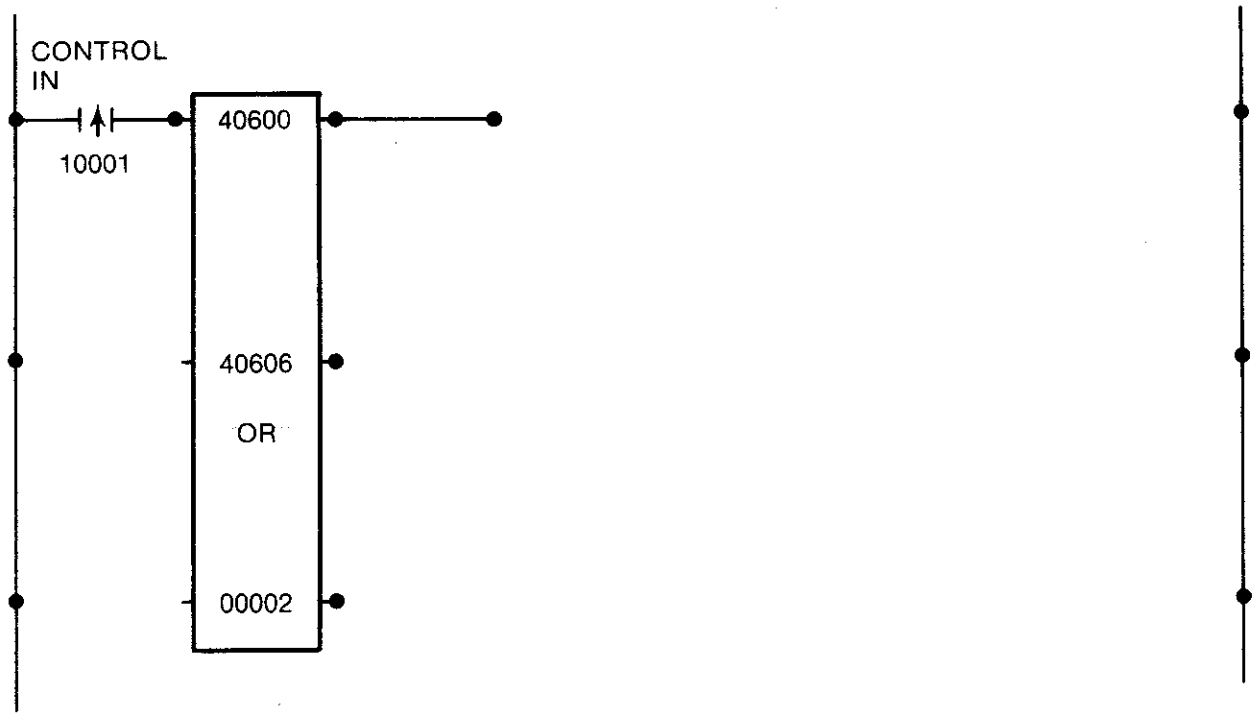
Top: Control in. Every scan this node is powered, the OR function is performed. A transitional contact should be used if single operations are desired.

Outputs

Top: Passes power when top input is powered.

OR

Network #55



SOURCE MATRIX

40600 = 1111111100000000	40601 = 1111111100000000

DESTINATION MATRIX BEFORE MOVE

40606 = 1111111111111111	40607 = 0000000000000000

DESTINATION MATRIX AFTER MOVE

40606 = 1111111111111111	40607 = 1111111100000000

Network Description

Whenever 10001 passes power, the bit matrix formed by registers 40600 and 40601 will be ORed with the bit matrix formed by 40606 and 40607. The result of this operation will be copied into registers 40606 and 40607.

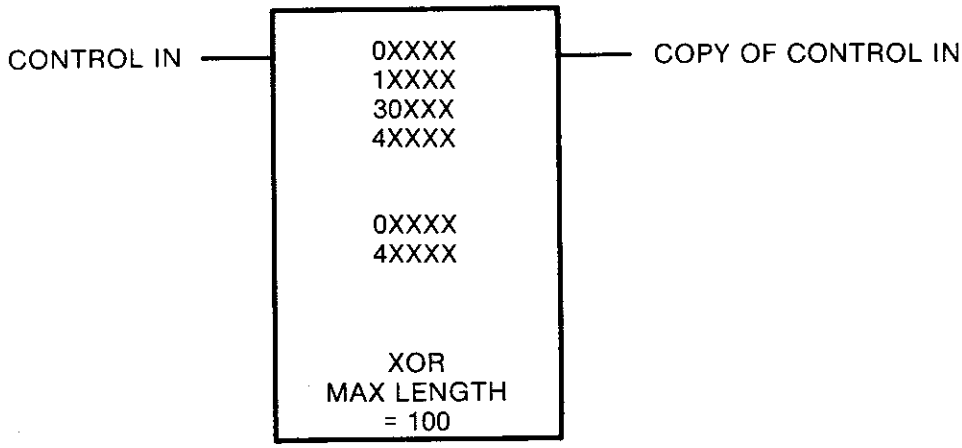
WARNING: The destination for this function can be a group of outputs. This function will override any disabled coils within this group without enabling them.

CAUTION: Outputs cannot be turned off with this function.

EXCLUSIVE OR

This function logically "xors" each bit in a source matrix with its corresponding bit in a second (destination) matrix. If either bit is a "1", the bit in the destination matrix will be set to a "1". If both bits are a "1" or a "0", the bit in the destination matrix will be cleared to a "0". A truth table follows:

Bit 1 Source	Bit 1 Destination Before Move	Bit 1 Destination After Move
0	0	0
0	1	1
1	0	1
1	1	0



Function Block

The top node is the data source and can be one of the following:

- the first 0XXXX reference number in a table of output references
- the first 1XXXX reference number in a table of input references
- the first 30XXX reference number in a table of input registers
- the first 4XXXX reference number in a table of holding registers.

The middle node is the destination and can be one of the following:

- the first 0XXXX reference number in a table of output references
- the first 4XXXX reference number in a table of holding registers.

The bottom node contains the symbol XOR and a number specifying table length. Maximum table length = 100 (maximum number of bits in matrix = 1600)

Inputs

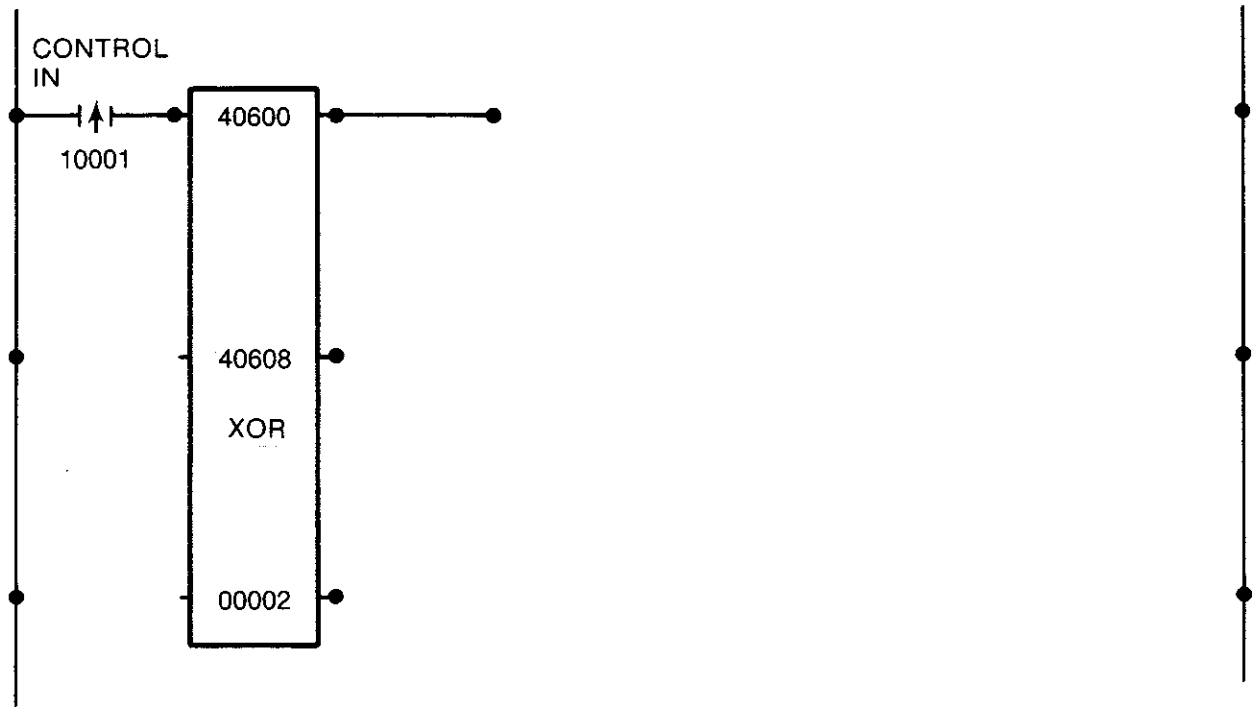
Top: Control in. Every scan this node is powered, the XOR function is performed. A transitional contact should be used if single operations are desired.

Outputs

Top: Passes power when top input is powered.

EXCLUSIVE OR

Network #56



SOURCE MATRIX

40600 = 1111111100000000	40601 = 1111111100000000

DESTINATION MATRIX BEFORE MOVE

40608 = 1111111111111111	40609 = 0000000000000000

DESTINATION MATRIX AFTER MOVE

40608 = 0000000011111111	40609 = 1111111100000000

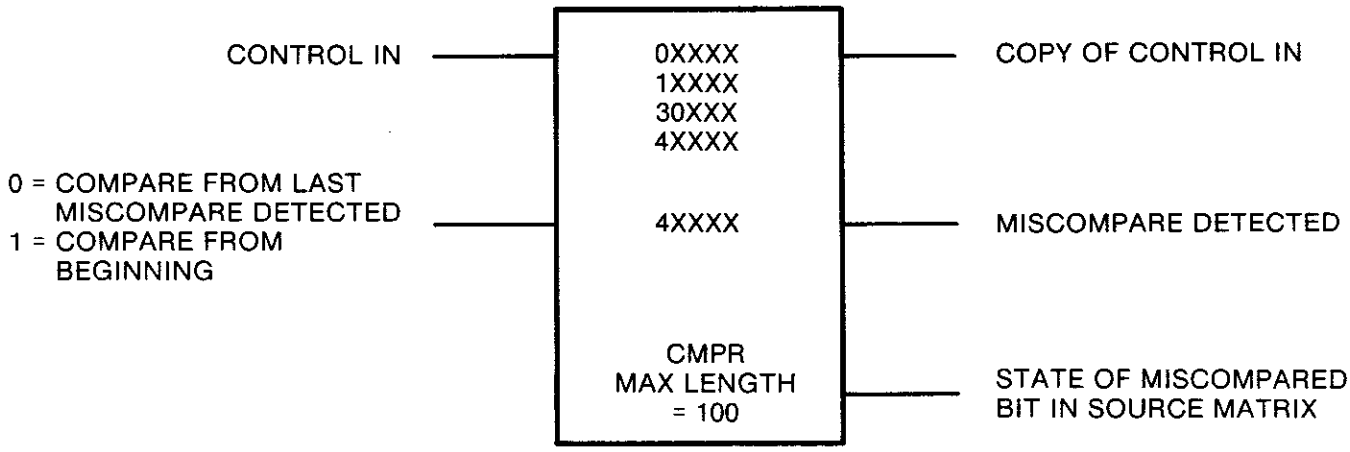
Network Description

Whenever 10001 passes power, the bit matrix formed by registers 40600 and 40601 will be exclusive ORed with the bit matrix formed by 40608 and 40609. The result of this operation will be copied into registers 40608 and 40609.

WARNING: The destination for this function can be a group of outputs. This function will override any disabled coils within this group without enabling them.

COMPARE

This function compares the bit pattern of one matrix against the bit pattern of a second matrix for discrepancies.



Function Block

The top node is the data source (matrix "A") and can be one of the following:

- the first 0XXXX reference number in a table of output references
- the first 1XXXX reference number in a table of input references
- the first 30XXX reference number in a table of input registers
- the first 4XXXX reference number in a table of holding registers.

The middle node must be a holding register (4XXXX). This register is the pointer. It will display the miscompared bit number. The next consecutive register (4XXXX +1) is the start of the table which the source table will be compared against (matrix "B").

The bottom node contains the symbol CMPR and a number specifying table length. Maximum table length = 100 (maximum number of bits in matrix = 1600)

Inputs

Top: Control in. Every scan this node is powered, the compare function is performed. A transitional contact should be used if single operations are desired.

Middle: When powered, the search for miscompares starts at the beginning of the matrices. When not powered, the search for miscompares starts with the next bit after the previous miscompare.

Outputs

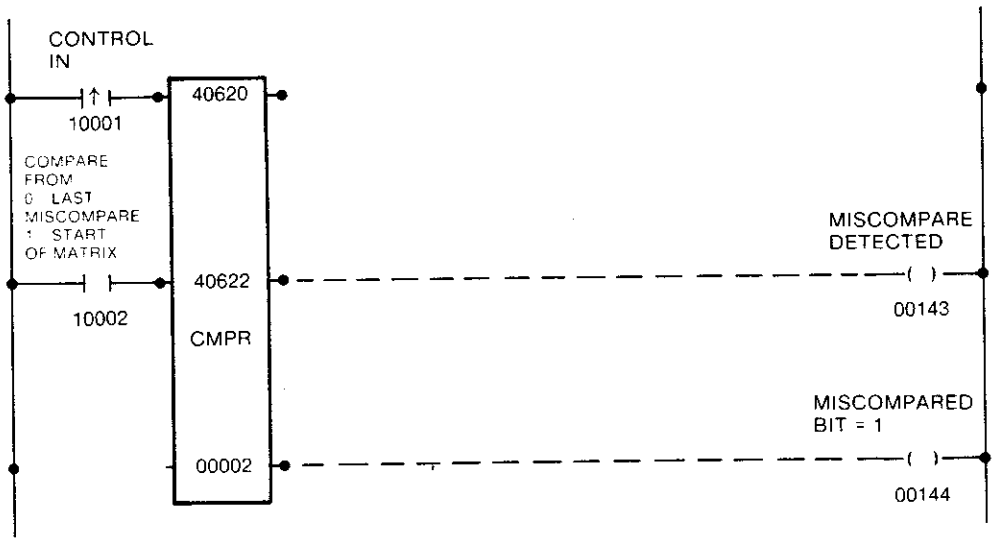
Top: Passes power when top input is powered.

Middle: Passes power when a miscompare is detected and the top input is powered

Bottom: Passes power if the miscompared bit = "1" in the source (matrix "A") and the top input is powered

COMPARE

Network #58



POINTER
40622

MATRIX "A"

40620	= 0000 0000 0000 0000
40621	= 1000 0000 0000 0001

MATRIX "B"

40623	= 0000 0000 0000 0000
40624	= 0000 0000 0000 0000

Network Description

If 10002 is energized, then every scan the "Control In" node receives power, matrix "A" will be compared against matrix "B", which has all bits cleared to "0". This comparison is done bit-by-bit. If a bit in matrix "A" = a bit in matrix "B", both "0's" or both "1's", then the next two bits are compared. In the network above, this bit-by-bit comparison would continue until bit 17. At this point, because the two bits are not the same (matrix "A" = 1, matrix "B" = "0"):

the function stops
Pointer register, 40623 = 17
Energize 00143 for one scan
Energize 00144 for one scan

If 10002 is de-energized, the 1st transition of 10001 will:

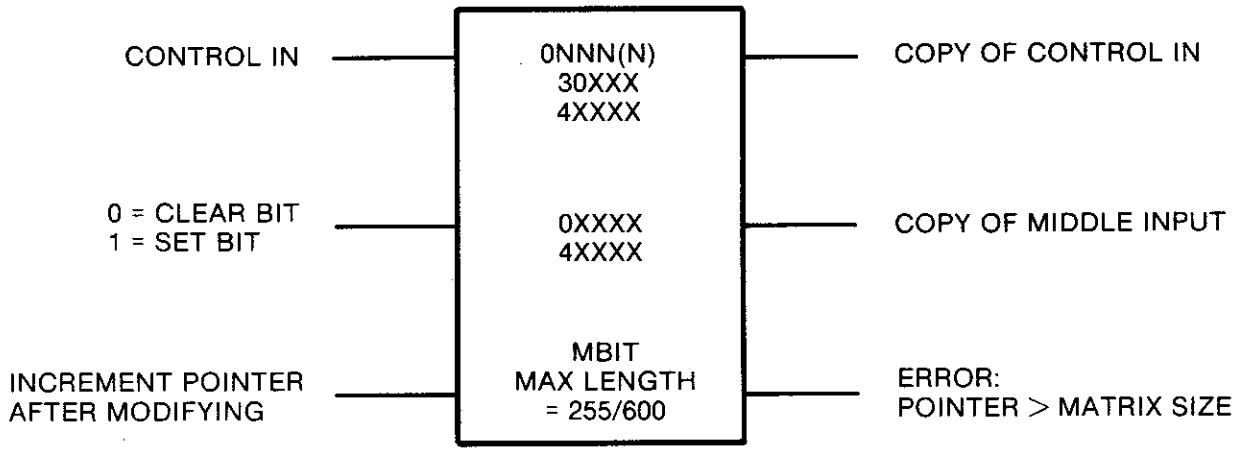
Stop the function
Pointer register, 40623 = 17
Energize 00143 for one scan
Energize 00144 for one scan

The 2nd transition of 10001:

Stop the function
Pointer register, 40623 = 32
Energize 00143 for one scan
Energize 00144 for one scan

BIT MODIFY

The function alters a specific bit within a matrix.



Function Block

The top node is the pointer and can be one of the following:

- A decimal number ranging from 1 to 4080 in 16 bit CPU's or 1 to 9600 in 24 bit CPU's
- An input register (30XXX)
- A holding register (4XXXX)

The middle node can be one of the following:

- The first 0XXXX reference number in a table of output references
- The first 4XXXX reference number in a table of holding registers

The bottom node contains the symbol MBIT and a number specifying table length. Table length may range from:

1 to 255 in 16 bit controllers
1 to 600 in 24 bit controllers

Inputs

Top: Control in. Every scan this node is powered, the bit modify function is performed. A transitional contact should be used if single operations are desired.

Middle: When powered, the "control in" input will cause the bit number specified in the top node to be set to a "1"

When not powered, the "control in" input will cause the bit number specified in the top node to be cleared to a "0"

Bottom: When powered, and if the pointer is a holding register (4XXXX), the pointer will increment each scan the top input receives power.

Outputs

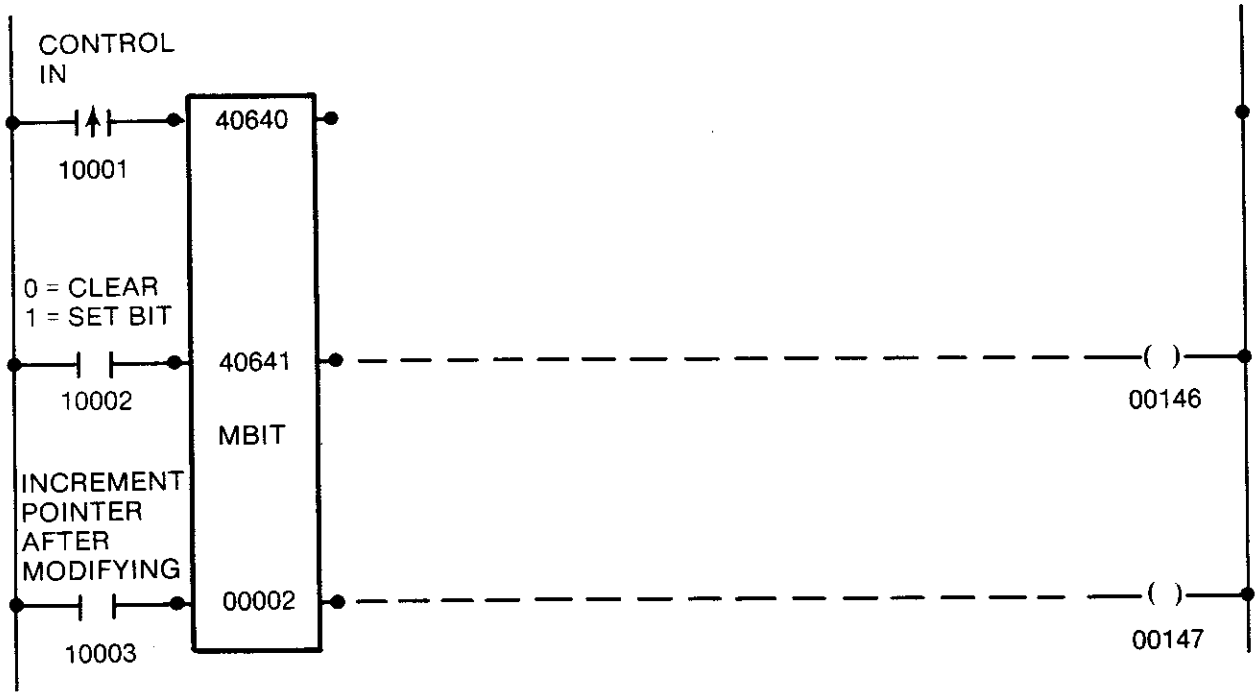
Top: Passes power when top input is powered

Middle: Passes power when the top and middle inputs are present

Bottom: Error. Passes power if the pointer value is > the matrix size

BIT MODIFY

Network #60



POINTER

40640

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	= BIT #
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 40641
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 40642
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	= BIT #

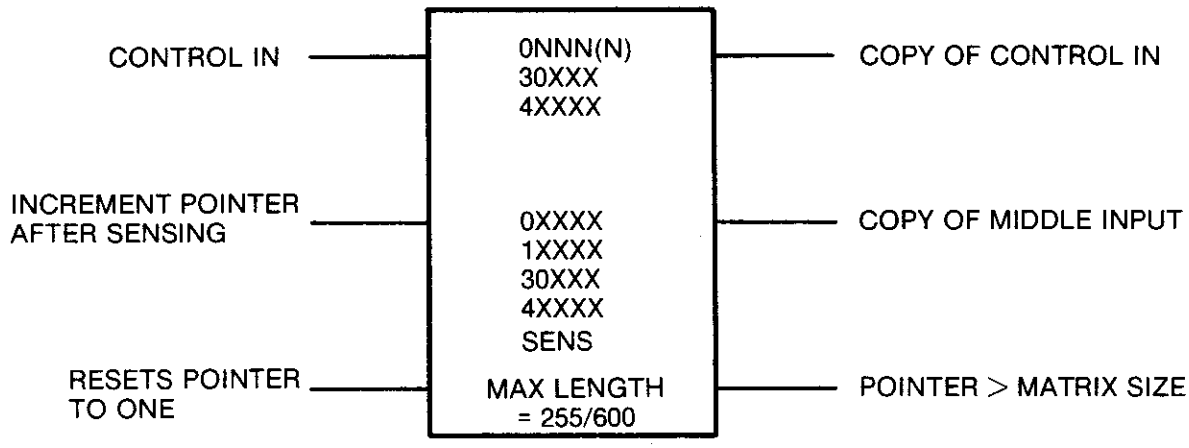
Network Description

If register 40640 = 16, and 10002 is closed, then, when 10001 transitions from off to on, bit #16 in register 40641 would be set to a "1", and coil 00146 would be energized for one scan. If 10003 had been closed the pointer value in register 40640 would have incremented to 17.

WARNING: The destination for this function can be a group of outputs. This function will override any disabled coils within this group without enabling them.

BIT SENSE

This function determines the sense, "1" or "0", of specific bit within a matrix.



Function Block

The top node is the pointer and can be one of the following:

- A decimal number ranging (1 to 4080 in 16 bit CPU's or 1 to 9600 in 24 bit CPU's)
- A input register (30XXX)
- A holding register (4XXXX)

The middle node can be one of the following:

- The first 0XXXX reference number in a table of output references
- The first 1XXXX reference number in a table of input references
- The first 30XXX reference number in a table of input registers
- The first 4XXXX reference number in a table of holding registers

The bottom node contains the symbol sens and a number specifying table length. Table length may range from:

1 to 255 in 16 bit controllers
1 to 600 in 24 bit controllers

Inputs

Top: Control in

Middle: When powered, and if the pointer is a holding register (4XXXX), the pointer will increment each scan the top input receives power. If the pointer is incremented to the end of the table, it will automatically reset to one and continue incrementing.

Bottom: When powered, and if the pointer is a holding register (4XXXX), resets pointer value to 1. A transitional contact should be used if a single reset is desired.

Outputs

Top: Passes power when top input is powered

Middle: Passes power if the bit number specified by the pointer value = "1"

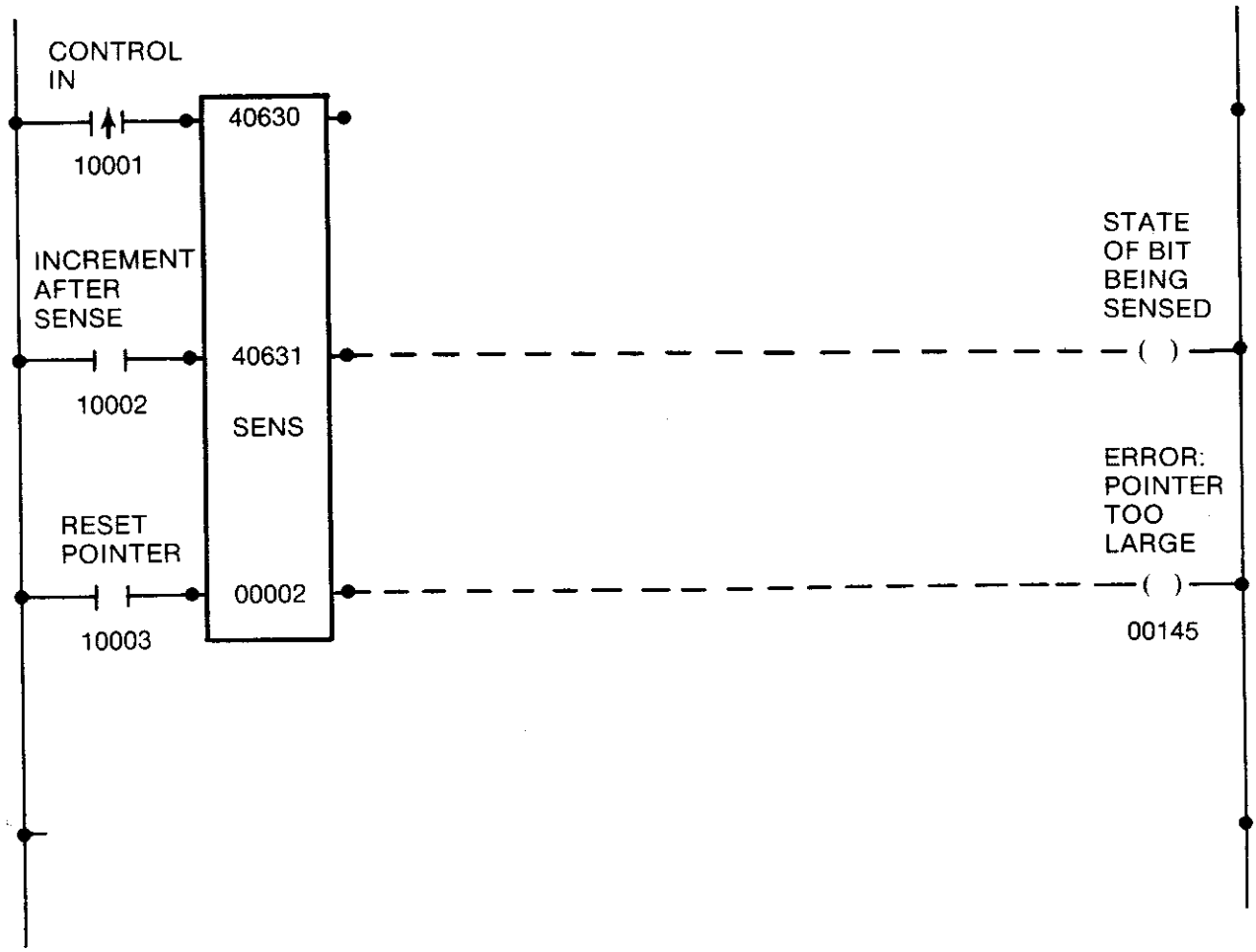
Bottom: Passes power if the pointer value is > the matrix size

If the middle node entry specifies coils, the controller erroneously marks those coils as used, and prevents their proper use elsewhere in the user program. If the coil reference is changed to a different coil reference or a register reference, then the original coils are freed for additional use.

If the middle node entry specifies inputs, then coils numbered with the same last four digits are erroneously marked as used, and are unavailable for proper use elsewhere in the program. If, for example, input reference 10017 is specified in the middle node, then coils 00017 — 00032 are erroneously marked as used.

BIT SENSE

Network #59



POINTER

40640

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	= BIT #
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	= 40641
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 40642

Network Description

If register 40630 = 8, then, when 10001 transitions from off to on, coil 00145 will be on for one scan.

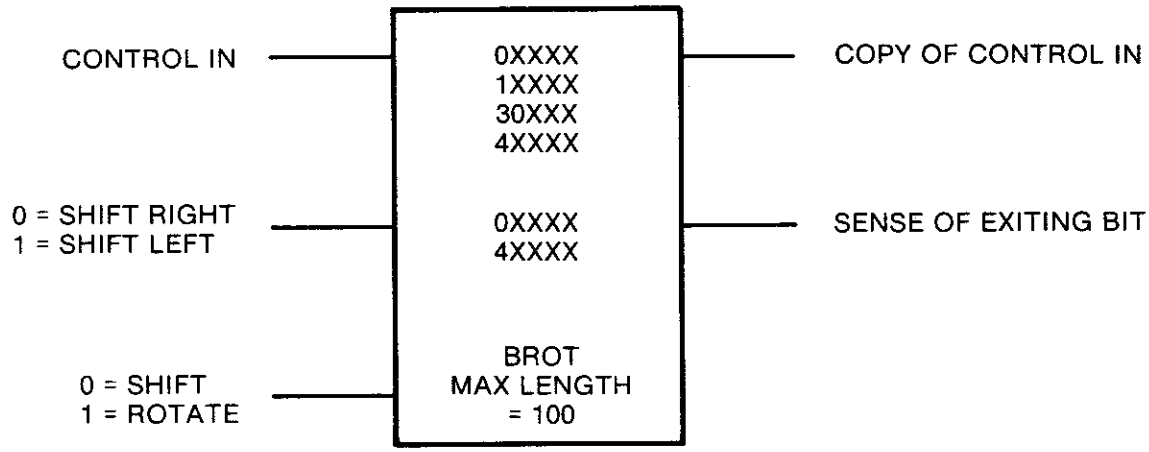
If 10002 had been closed when the above operation was performed, the pointer value in register would have incremented to 9.

If 10003 had been closed when the above operation was performed, the pointer would have been reset to 1.

If 10002 and 10003 had been closed when the above operation was performed, the pointer would have been reset to 1, then incremented to 2.

BIT ROTATE/SHIFT

This function rotates or shifts the bit pattern of a matrix.



Function Block

The top node can be one of the following:

- the first 0XXXX reference number in a table of output references
- the first 1XXXX reference number in a table of input references
- the first 30XXX reference number in a table of input registers
- the first 4XXXX reference number in a table of holding registers.

The middle node can be one of the following:

- the first 0XXXX reference number in a table of output references or (counts as the one time coil can be used)
- the first 4XXXX reference number in a table of holding registers.

The bottom node contains the symbol BROT and a number specifying table length. Maximum table length = 100 (maximum number of bits in matrix = 1600).

Inputs

Top: Control in every scan this node is powered, the bit rotate function is performed. A transitional contact should be used if single operations are desired.

Middle: When powered, the "control in" input will cause the entire matrix to shift one bit to the right

When not powered, the "control in" input will cause the entire matrix to shift one bit to the left

Bottom: When powered, the "control in" input will cause a copy of the exiting bit to be placed at the opposite end of the matrix

When not powered, the "control in" input will cause a "0" to be placed at the opposite end of the matrix

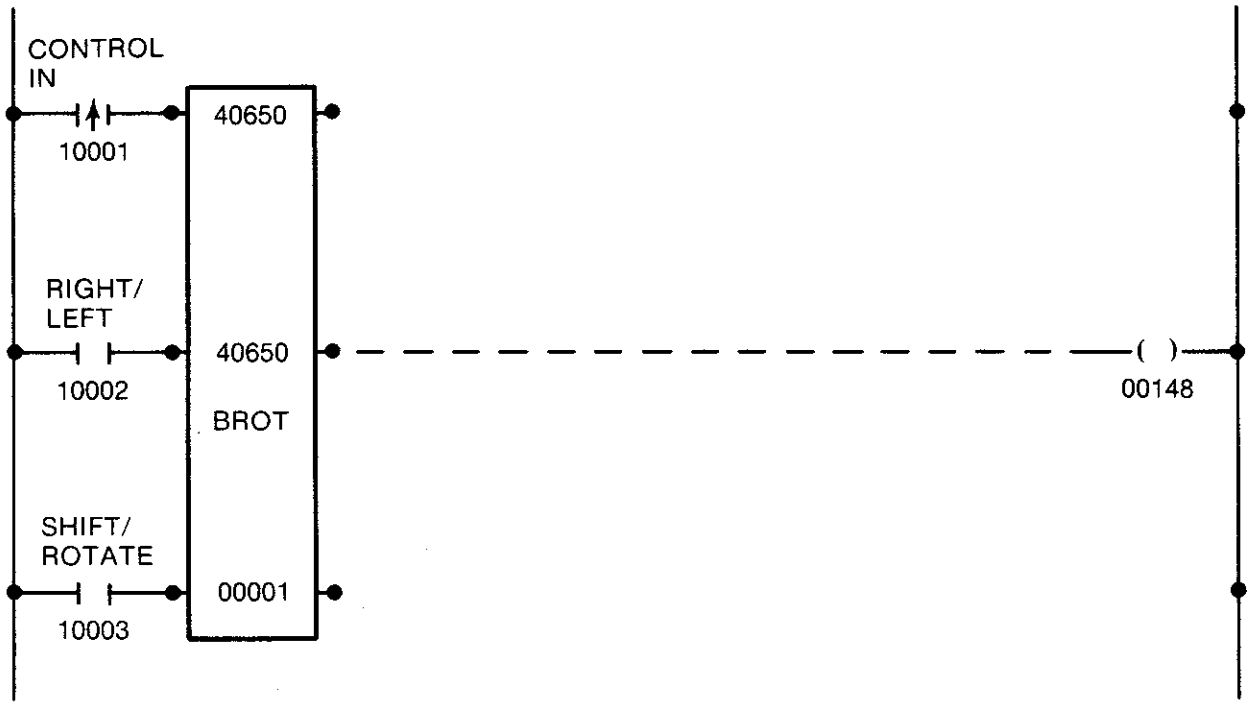
Outputs

Top: Passes power when top input is powered

Middle: Passes power if the exiting bit is a "1".

BIT ROTATE/SHIFT

Network #61



0000000000000101	=	BIT ROTATE RIGHT BEFORE "CONTROL IN"
1000000000000010	=	ABOVE AFTER "CONTROL IN"
0100000000000001	=	ABOVE AFTER SECOND "CONTROL IN"

Network Description

The first transition of 10001 will cause the bit pattern in register 40650 to shift one position to the right. Coil 00148 will be energized since the "exiting" bit will be a "1".

If 10003 had been on when the above operation was performed, then the "exiting" bit would have "rotated" to the start of the matrix (bit 1).

WARNING: The destination for this function can be a table of outputs (0XXXX). This function will override any disabled coils within this table without enabling them.

0XXXX Destinations

If the middle node entry for a data transfer function is an output reference number (0XXXX), it counts as the one time the referenced coils may be used.

Applies to:

Block Move (BLKM)
First Out (FOUT)
Complement (COMP)
Logical and (AND)
Logical or (OR)
Logical Exclusive or (XOR)
Bit Modify (MBIT)
Bit Sense (SENS)
Bit Rotate (BROT)

Examples

If any of the below function blocks were already programmed, then an attempt to program a coil with a reference number ranging from 00017 to 00048 would result in the P190 error message 'coil used".

Similarly, if any coil from 0017 to 00048 were already programmed, then an attempt to program any of the following function blocks would also result in the P190 error message "coil used".