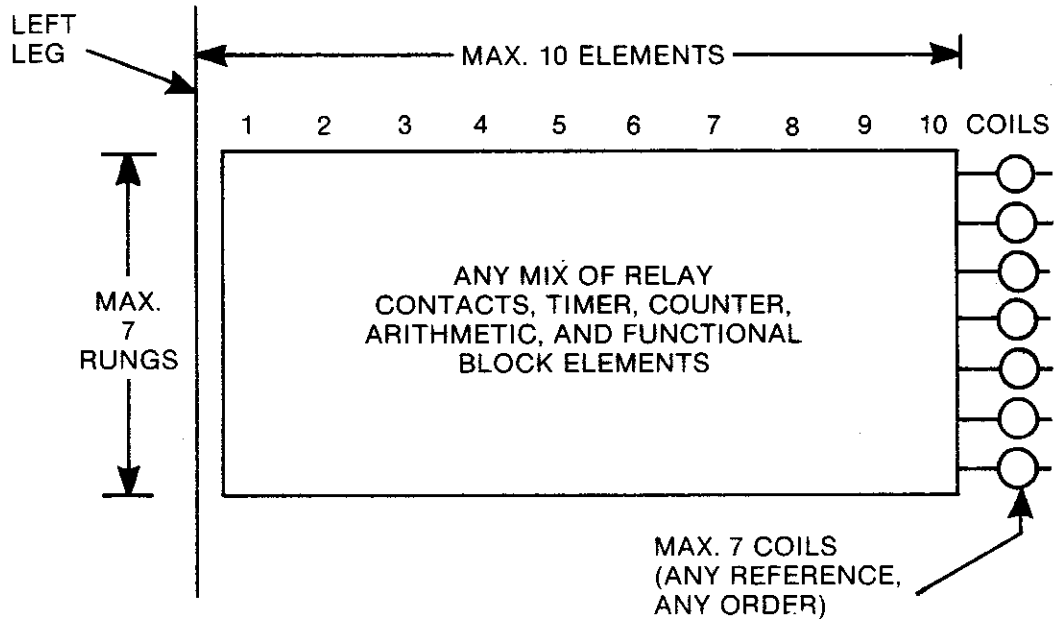
584 NETWORK STRUCTURE

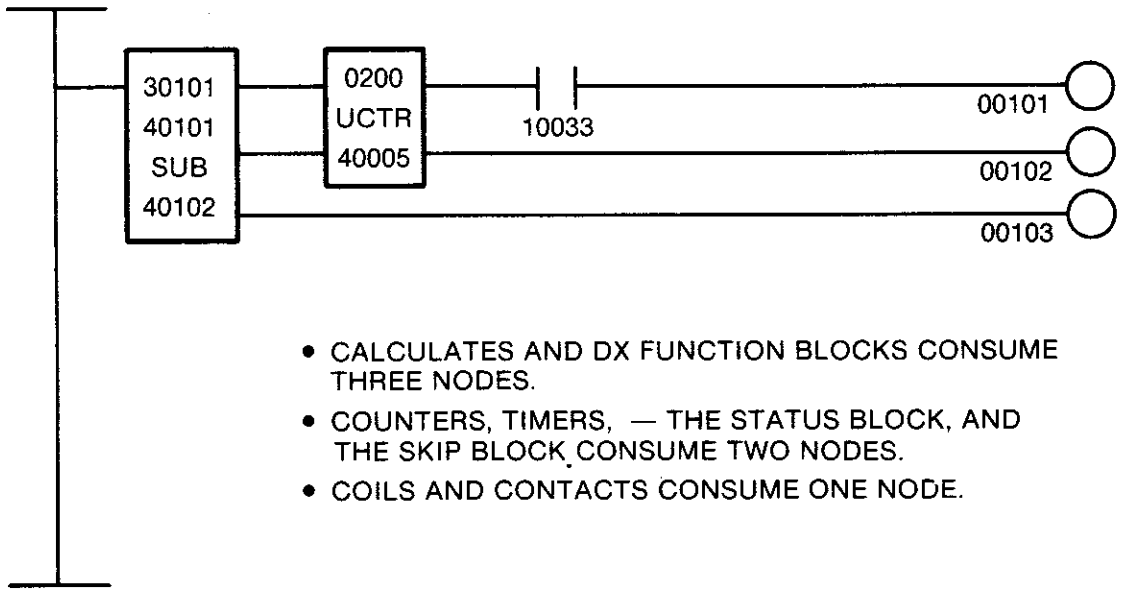
User logic is programmed using ladder logic symbology into "networks". Each network is a small ladder diagram, 7 rungs high, and 11 columns wide. This provides 77 positions within the network. Each of these positions is termed a "node". See General Network Format, below.

"Power" within the network "flows" from left to right, and vertically up or down. Power cannot flow from right to left. See Vertical Node Consumption, below.

Coils are automatically displayed in the 11th columns, however they are solved based on what node they were programmed in (where the dotted line starts).



General Network Format



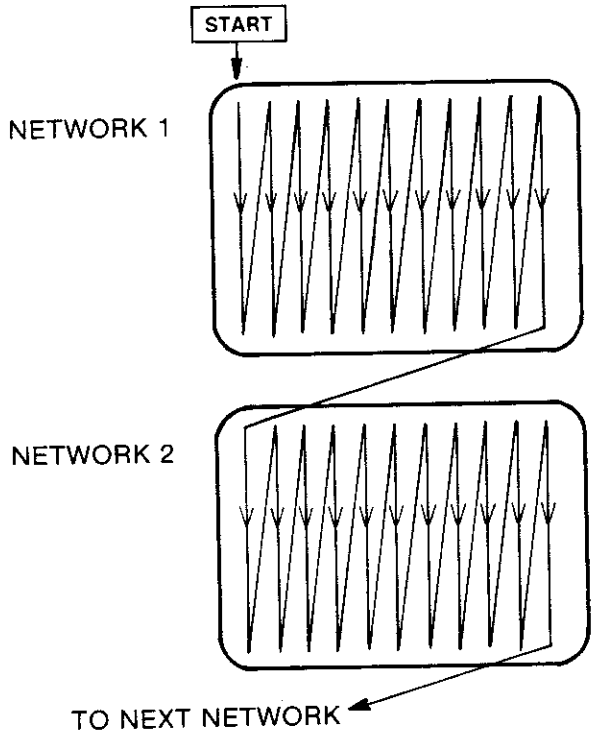
- CALCULATES AND DX FUNCTION BLOCKS CONSUME THREE NODES.
- COUNTERS, TIMERS, — THE STATUS BLOCK, AND THE SKIP BLOCK CONSUME TWO NODES.
- COILS AND CONTACTS CONSUME ONE NODE.

Vertical Node Consumption

LOGIC SOLVING SEQUENCE

Sequence

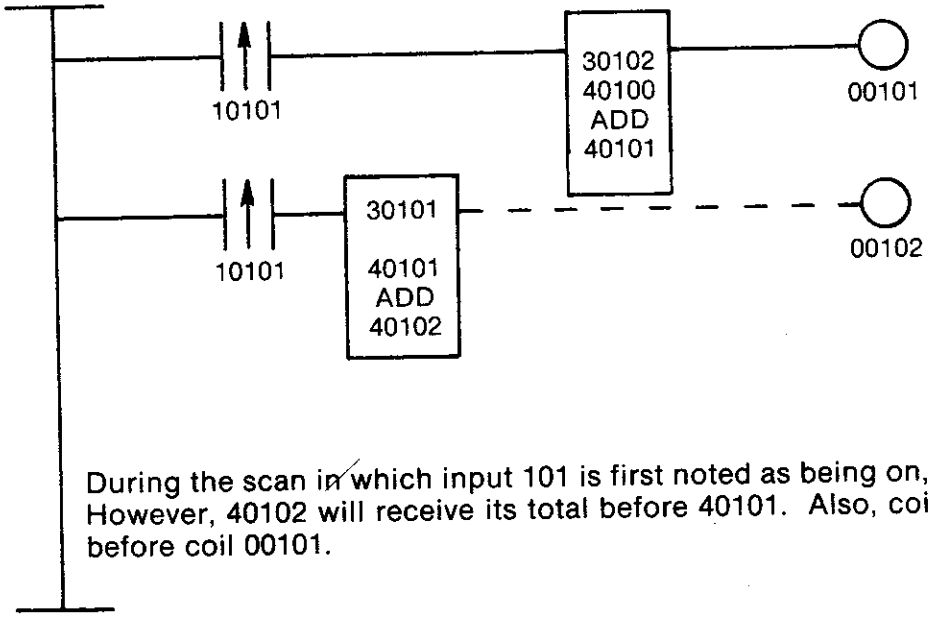
The user logic is solved column by column from left to right within each network.



THE 584 SOLVES ONE ELEMENT AT A TIME, TOP TO BOTTOM, LEFT TO RIGHT.

IF THE 584 IS STOPPED, OR LOSES POWER IN THE MIDDLE OF A NETWORK, THE LOGIC SOLUTION STARTS OVER FROM THE FIRST NETWORK WHEN POWER IS RESTORED TO THE CONTROLLER.

ELEMENT POSITIONAL RELATIONSHIPS

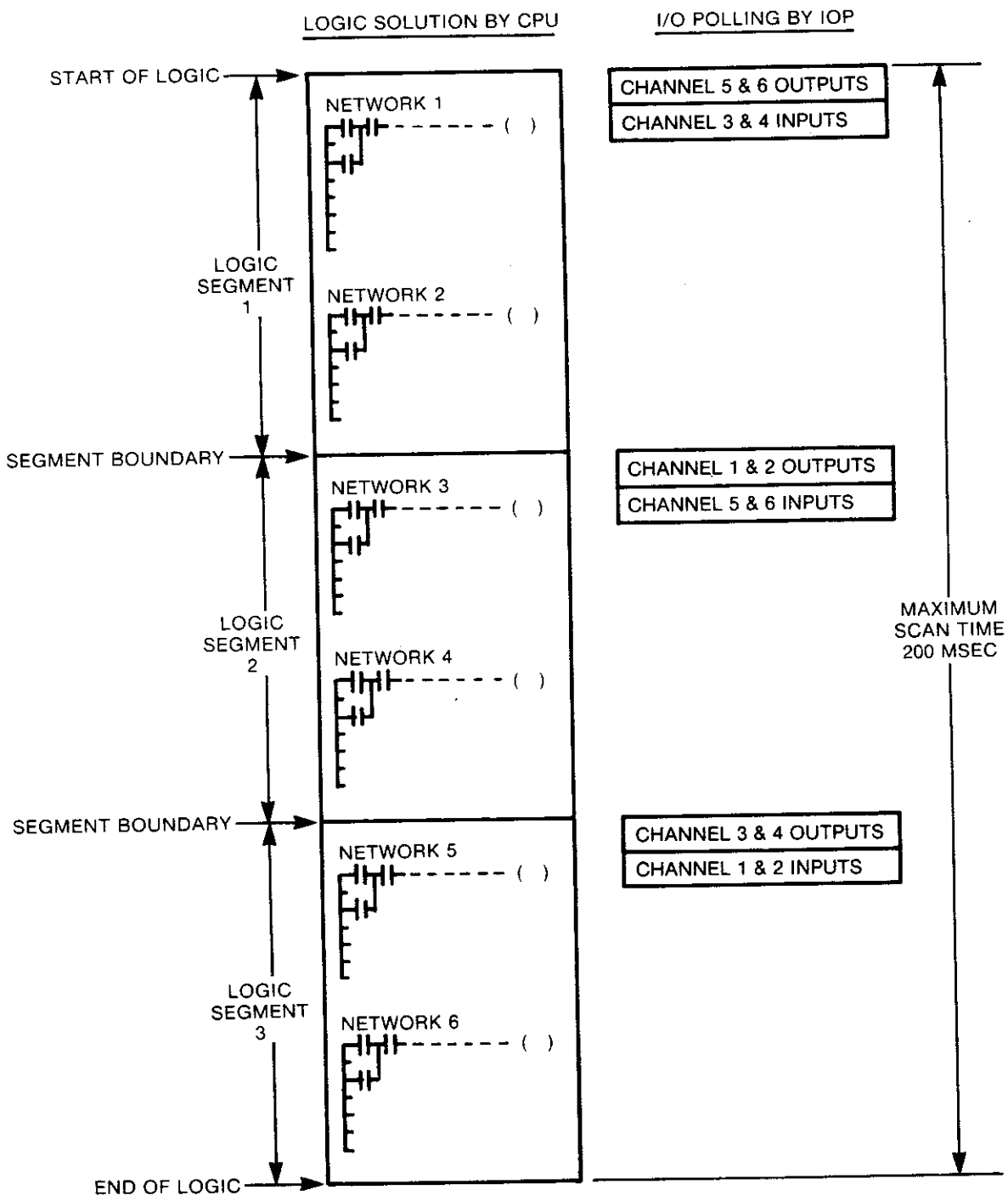


During the scan in which input 101 is first noted as being on, two adds take place. However, 40102 will receive its total before 40101. Also, coil 00102 will be solved before coil 00101.

LOGIC SOLUTION — I/O POLLING

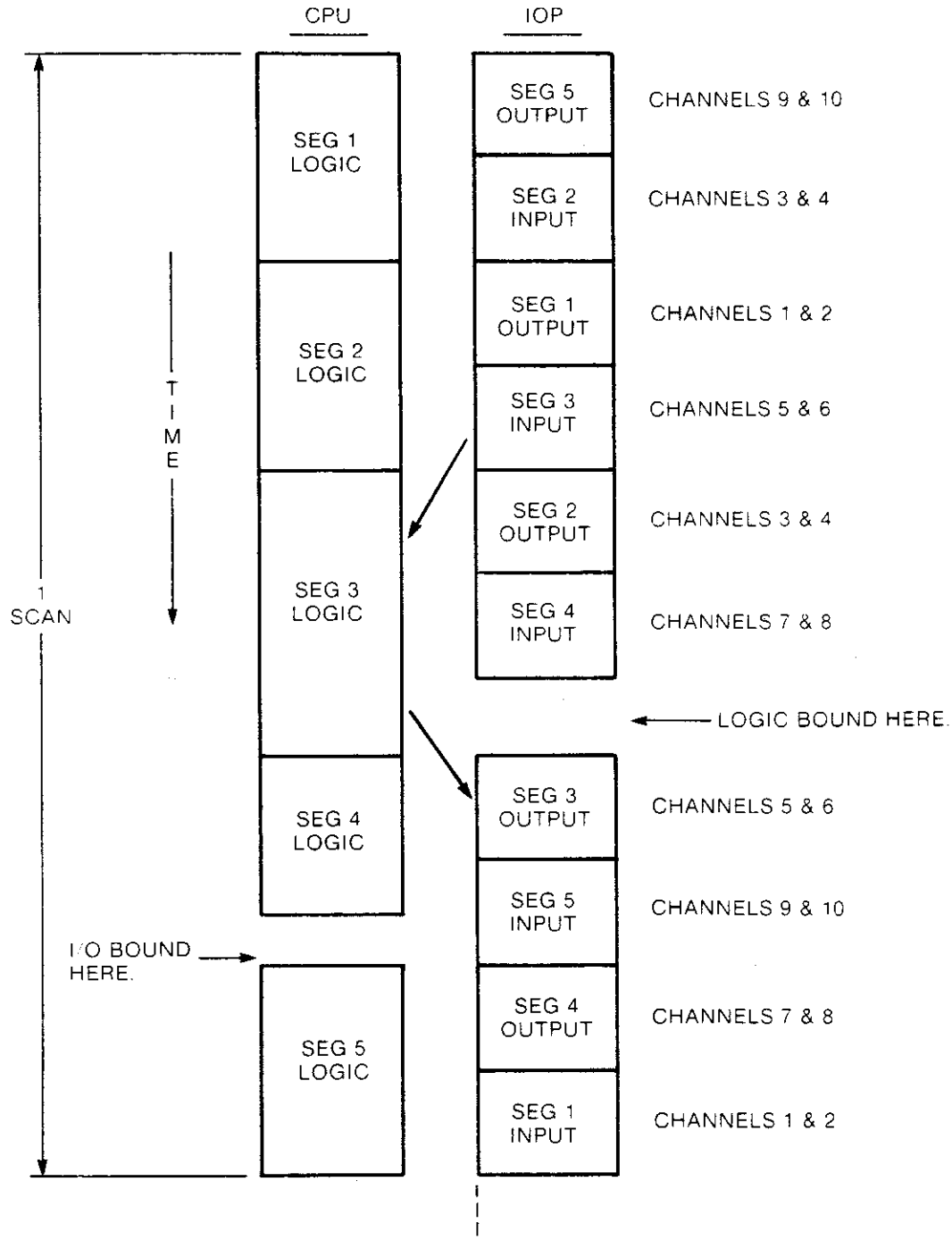
- The 584 provides a logic "segment" for each pair of channels which the system has been configured for, e.g., 32 channels = 16 logic segments.
- Each logic segment may contain as many networks as desired subject to memory constraints and a maximum scan time of 200 msecs.
- The 584 uses 2 processors; one solves user logic, while the other reads inputs and drives outputs.
- When the 584 is started, the run light is on and the solution of the user logic and I/O polling begins.
- The 584 solves user logic starting with network 1 and proceeds thru all networks sequentially, until the last network is solved.
- The process of reading all inputs, solving all logic, and driving outputs is termed a "scan".
- Maximum allowable scan time = 200 milliseconds.
- When the controller is running it will repeatedly scan until it is stopped.
- A scan starts with:
  1. The solution of network #1.
  2. Driving the outputs for the last pair of channels.
- Solution of logic within a network starts with the top left node and solves one element at a time, top to bottom, left to right.
- Coils are automatically displayed in the 11th column, however, they are solved based on what node they were programmed in (where the dotted line starts).

NOTE: THE EXAMPLE SHOWN BELOW IS FOR A 584 SYSTEM CONFIGURED FOR 6 CHANNELS, AND WITH 6 NETWORKS OF USER LOGIC.



SEGMENTATION

Segmentation is the utilization of two processors (1 to solve logic and the other to poll I/O) to greatly reduce the 584's scan time. One I/O segment = two channels: Seg 1 = Chan 1 & 2, Seg 2 = Chan 3 & 4, etc. A logic segment is provided by the 584 for each pair of channels the system has been configured for.

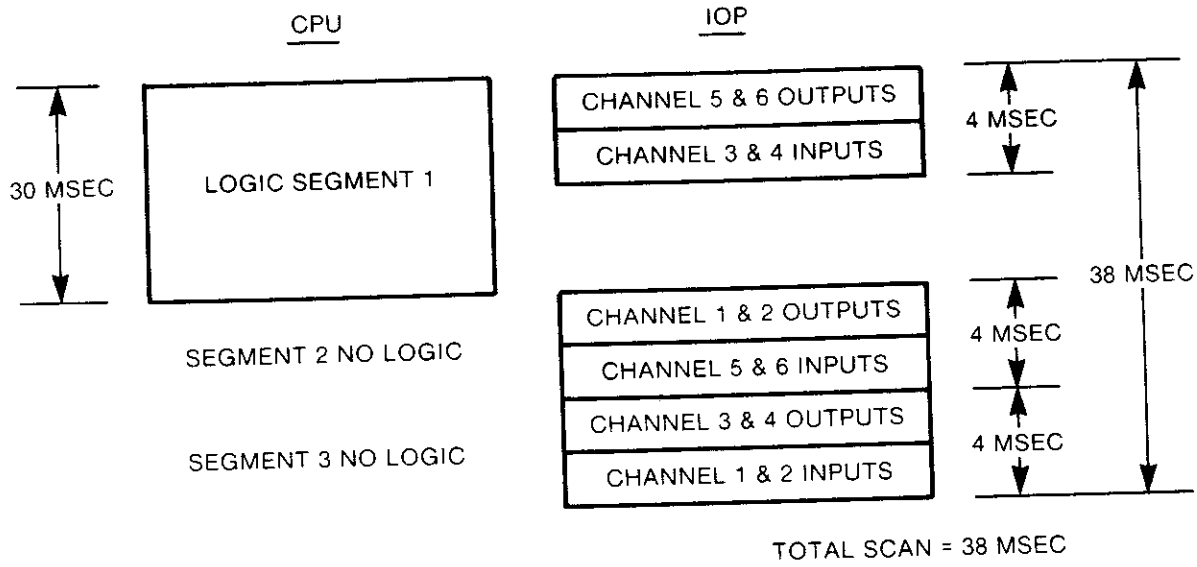


A TYPICAL 584 SYSTEM WILL BE LOGIC BOUND VS I/O BOUND

SEGMENTATION

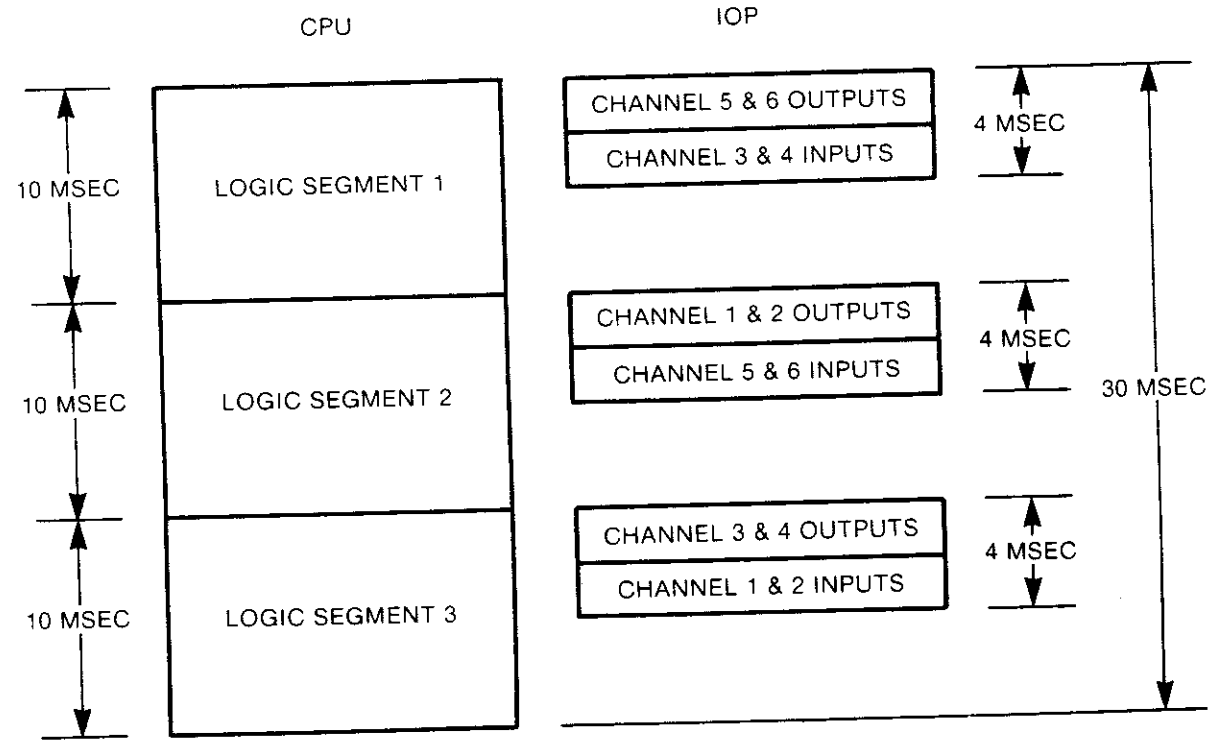
The following examples illustrate the differences in scan time for an identical channel system. Note that example two has a shorter scan time.

Example 1 — All Logic in One Segment



TOTAL SCAN = 38 MSEC

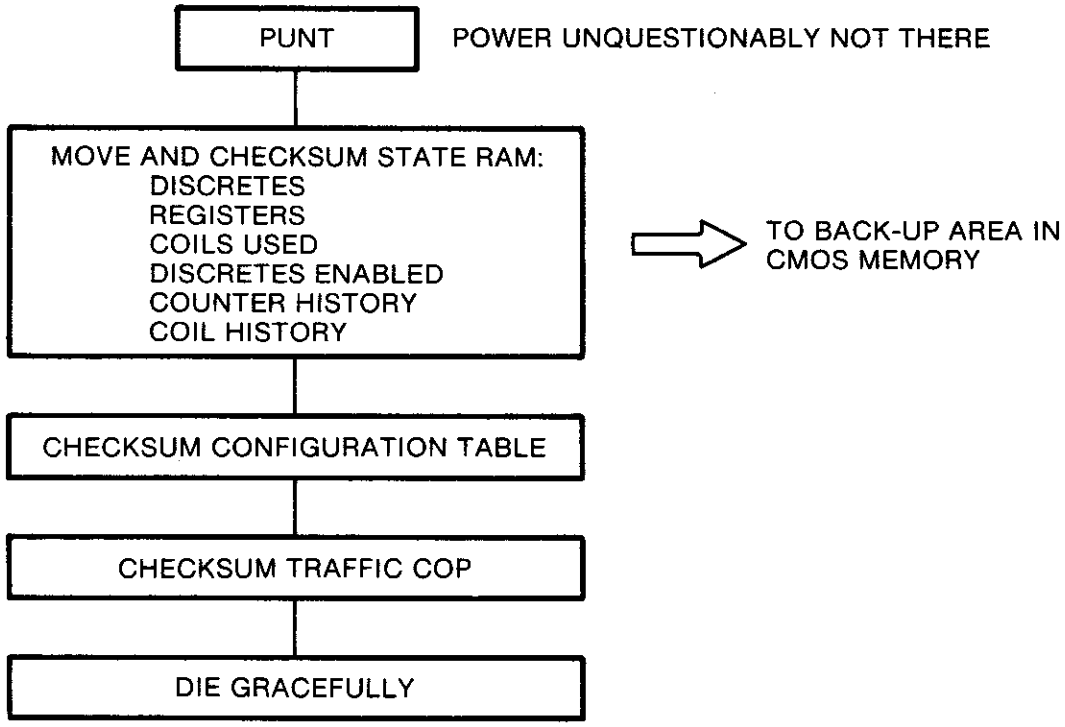
Example 2 — Logic Evenly Distributed Across All Segments



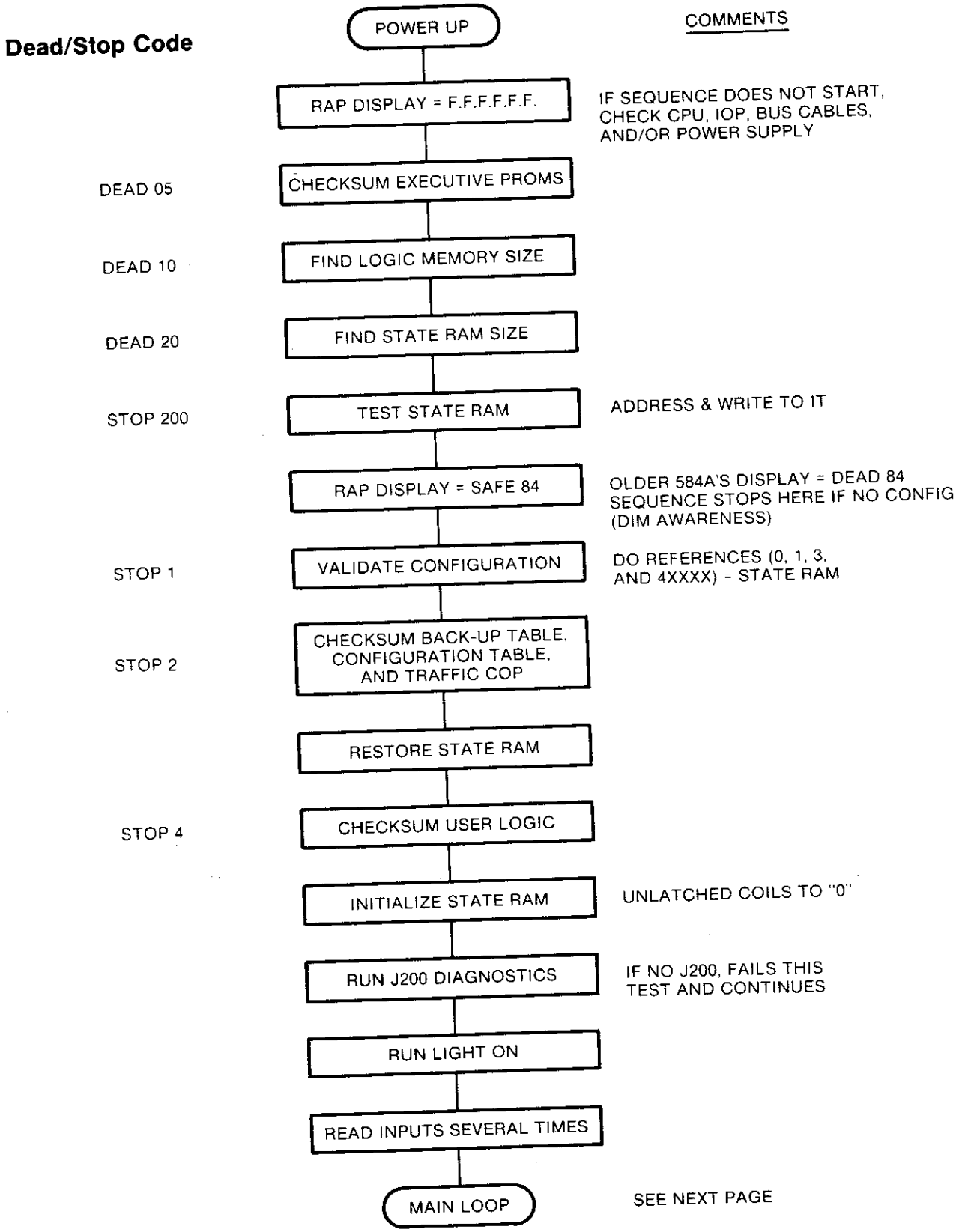
TOTAL SCAN = 30 MSEC

POWER LOSS

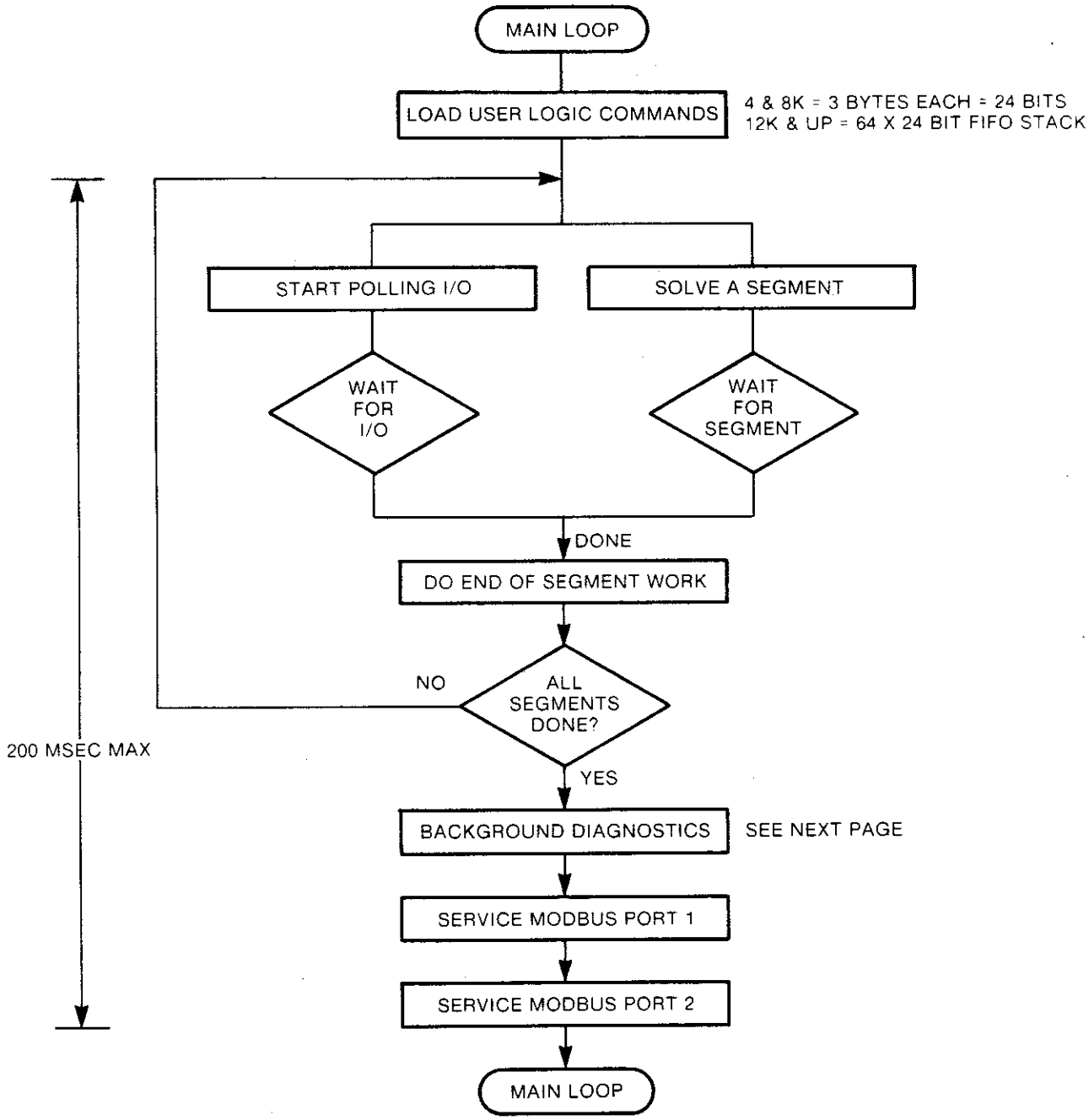
When the 584 detects "Power Unquestionably Not There" it performs a "PUNT" routine which moves the state RAM to the back-up area on the memory board, where it, along with user logic, ASCII messages, configuration table, and traffic cop are stored in battery powered CMOS memory.



POWER UP SEQUENCE



MAIN LOOP SEQUENCE



BACKGROUND DIAGNOSTICS

Performs one of following per scan:

1. Checksum executive proms (16 words per test)
2. Write/read memory test pattern (word each test to user logic and state RAM) 3 patterns each test
3. Hardware Logic Solver (HLS). 1 network with relays, coil, vertical and horizontal shorts.
4. J200 loopback/user logic checksum (4 words, 3 patterns) to J200. Checksum user logic while waiting.
5. Checksum loadable software module area (16 words per test).
6. Checks extended memory parity checker in 584L with extended memory.

HINTS TO MINIMIZE SCAN TIME

- Only configure the number of I/O channels that will be required. This will limit the number of program segments being solved.
- Keep in mind that the non-J200 I/O channels are four times slower than the J200 I/O (16 ms for 4 full channels local vs, 4 ms for 2 J200 drops).
- Distribute user logic evenly among the number of program segments configured in the system. Since 2 channels of I/O are serviced while a segment of logic is being solved, there is a fair amount of logic that can be solved without an impact on scan time.
- Leave unused slots in a channel inhibited to improve servicing time (applies to local I/O)
- Don't solve complex logic every scan if, say, 5 times per second will do just as well.
- Use the skip functions to bypass conditionally unnecessary logic. Remember that skip 0 is fastest of all. Skip 0 stops at the end of the segment.
- Small systems are usually I/O bound, medium and large systems are almost always logic bound. Focus your attention accordingly.

SOLVE TIME SPECIFICATIONS

All times are specified in microseconds, unless otherwise noted.

Function	584A		584M		584L	
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum
START NETWORK		4.51		4.51		
NO,NC,—,OPEN		0.26		0.26		
↑ TRANSITION		5.80		5.80		
↓ TRANSITION		5.55		5.55		
COIL (ENABLED)		8.32		8.32		
COIL (DISABLED)		5.28		5.28		
UCTR	13.09	13.97	13.09	13.97	13.09	13.97
DCTR	13.09	13.97	13.09	13.97	13.09	13.97
TIMER	8.05	9.56	8.05	9.56	8.05	9.56
ADD	9.59	10.85	9.59	10.85	9.59	10.85
SUB	9.59	11.10	9.59	11.10	9.59	11.10
MUL	9.59	63.58	9.59	63.58	9.59	63.58
DIV	9.59	116.50	9.59	116.50	9.59	116.50
R→T	140.00	200.00	140.00	200.00	12.50	15.75
T→R	147.00	208.00	147.00	208.00	13.00	16.50
T→T	156.50	206.00	156.50	206.00	13.25	17.00
BLKM	133.00	317.50	133.00	317.50	9.75	137.50
FIN	135.00	189.00	135.00	189.00	14.25	19.25
FOUT	162.00	188.50	162.00	188.50	16.00	17.25
SRCH	141.00	1809.00	141.00	1809.00	13.25	163.50
STAT	128.50	704.00	128.50	704.00	10.75	241.50
AND	143.00	852.00	143.00	852.00	9.75	210.00
OR	143.00	850.00	143.00	850.00	10.25	210.50
XOR	207.50	854.00	207.50	854.00	12.00	212.25
COMP	143.00	1167.00	143.00	1167.00	11.75	212.00
CMPR	140.00	2137.50	140.00	2137.50	10.75	284.00
MBIT	234.00	362.00	234.00	362.00	10.50	31.50
SENS	230.00	358.50	230.00	358.50	13.00	25.00
BROT (RIGHT)	143.00	3101.00	143.00	3101.00	11.75	216.25
BROT (LEFT)	143.00	3101.00	143.00	3101.00	11.75	215.75
READ	3 MSEC	6 MSEC	3 MSEC	6 MSEC	3 MSEC	6MSEC
WRIT	3 MSEC	6 MSEC	3 MSEC	6 MSEC	3 MSEC	6 MSEC
XMRD						
XMWT						
PID	0.5 MSEC	1.0 MSEC	0.5 MSEC	1.0 MSEC	0.5 MSEC	1.0 MSEC

SOLVE TIME SPECIFICATIONS

Overhead Functions

End of each segment	1.2 msec
End of logic — No MODBUS or RAP activity	1.9 to 2.2 msec
— with MODBUS activity	
Program 1 register	1.3 msec
Read 1 register	1.0 msec
Program 16 registers	2.15 msec
Read 16 registers	1.7 msec
Write 64 coils	1.59 msec
Read 64 coils	3.0 msec
Write 16 coils	1.59 msec
Read 16 coils	1.8 msec
Register Access Panel (RAP)	
Discrete status — 0XXXX	199 usec
1XXXX	203 usec
Register value — 3XXXX	199 usec
4XXXX	195 usec
Display 000584	15 usec
Memory location	63 usec
Port parameter	180 usec

Typical I/O Servicing Times

	Inputs	Outputs
1 Channel local I/O active	2.0 msec	2.0 msec
2 Channels local I/O active	4	4
1 Channel remote I/O active	1.3	1.4
2 Channels remote I/O active	1.3	1.3