SECTION IV
INTERNAL PRINCIPLES AND AUXILIARY EQUIPMENT

4.1 THEORY OF OPERATION

4.1.1 Introduction

The power and flexibility of the MODICON 184/384 Controller is provided by its software — or executive — capabilities. The 184/384 Controller has had broad acceptance in a large number of applications, but its potential in terms of a control system, not just relay replacement, has barely been tapped.

The following are descriptions of the system software data base (as of this writing) and includes a description of the I/O allocation tables and conventions designed by MODICON for proper system operation. Also provided is a description of the procedures required to properly integrate the Controller into a data processor system.

This information will normally NOT be required for the designer to program the Controller. The designer enters his program by means of the simple MODICON four-element logic lines. However, when the Controller is to be interfaced to a computer system, this information will assist the user in obtaining the data he requires. The specific core addresses for logic lines, registers, etc., are unique to each MOPS/TEF and are available from the MODICON Service Center.

Designer comments are always welcome, and the MODICON engineering and programming staff are available to aid the user in solving control design problems.

4.1.2 Scan

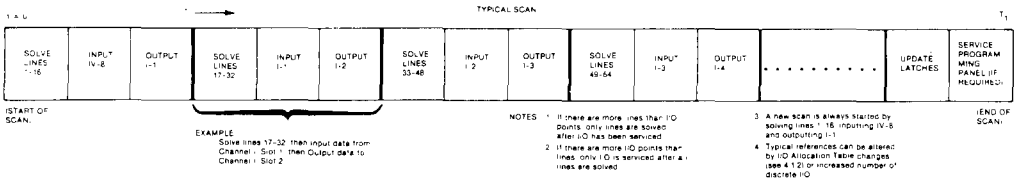
The MODICON 184/384 Controller processes its logic data by solving lines in numerical order, beginning with line 1 and continuing until the last line of the executive is solved. This completes one scan. As soon as one scan is completed, the next scan begins, again with line 1.

Each line is independently solved from element A to element D. The new results from each logic line (either coil status or data in registers) is immediately available for use by the next logic line. The scanning technique is very basic to the operation of the 184/384 Controller and should be understood before proceeding.

During the solving of logic lines, individual input and output modules are serviced by the Processor. Every line is solved once each scan and each I/O module serviced once each scan. The exact time to complete a scan varies from application to application, but depends on the number of logic lines scanned, the number of I/O provided, and the types of logic lines utilized.

NOTE

When power is supplied, a power-up sequence is performed which requires 500 ms. After this sequence, scanning is performed, based on real data (inputs and latches updated), beginning at line 1. If a power failure is detected, scanning is terminated at whichever line is currently being solved and the power-down sequence is initiated, which includes turning all outputs OFF.



SAMPLE SCAN

Lines	INPUT Channel	INPUT Typical Reference	OUTPUT Channel	OUTPUT Typical Reference
1-16	IV-8	3016	I-1	0001-0016
17-32	I-1	1001-1016	I-2	0017-0032
33-48	I-2	1017-1032	I-3	0033-0048
49-64	I-3	1033-1048	I-4	0049-0064
65-80	I-4	1049-1064	I-5	0065-0080
81-96	I-5	1065-1080	I-6	0081-0096
97-112	I-6	1081-1096	I-7	0097-0112
113-128	I-7	1097-1112	I-8	0113-0128
129-144	I-8	1113-1128	II-1	0129-0144
145-160	II-1	1129-1144	II-2	0145-0160
161-176	II-2	1145-1160	II-3	0161-0176
177-192	II-3	1161-1176	II-4	0177-0192
193-208	II-4	1177-1192	II-5	0193-0208
209-224	II-5	1193-1208	II-6	0209-0224
225-240	II-6	1209-1224	II-7	0225-0240
241-256	II-7	1225-1240	II-8	0241-0256
257-272	II-8	1241-1256	III-1	4001
273-288	III-1	3001	III-2	4002
289-304	III-2	3002	III-3	4003
305-320	III-3	3003	III-4	4004
321-336	III-4	3004	III-5	4005
337-352	III-5	3005	III-6	4006
353-368	III-6	3006	III-7	4007
369-384	III-7	3007	III-8	4008
385-400	III-8	3008	IV-1	4009
401-416	IV-1	3009	IV-2	4010
417-432	IV-2	3010	IV-3	4011
433-448	IV-3	3011	IV-4	4012
449-464	IV-4	3012	IV-5	4013
465-480	IV-5	3013	IV-6	4014
481-496	IV-6	3014	IV-7	4015
497-512	IV-7	3015	IV-8	4016
513-528	None	None	None	None
529-544	↓	↓	↓	↓
545-560	↓	↓	↓	↓
561-576	↓	↓	↓	↓
577-592	↓	↓	↓	↓
593-608	↓	↓	↓	↓
609-624	↓	↓	↓	↓
625-640	↓	↓	↓	↓
641-656	↓	↓	↓	↓
657-672	↓	↓	↓	↓
673-688	↓	↓	↓	↓
689-704	↓	↓	↓	↓
705-720	↓	↓	↓	↓
721-736	↓	↓	↓	↓
737-752	↓	↓	↓	↓
753-768	↓	↓	↓	↓
769-784	↓	↓	↓	↓
785-800	None	None	None	None

Table 20. Sample Scan

Table 20 illustrates the specific order of input/output servicing. After a group of 16 lines is solved, an input module is sampled with its data stored in the I/O status area of core memory, and status is provided to an output module. If, after all the I/O modules are serviced, there are lines to be solved, only the lines are solved and no I/O servicing is done. If there are fewer logic lines than I/O points, then only I/O modules are serviced after all lines are solved. Thus, the solving of lines and the servicing of inputs/outputs are accomplished once per scan, and always starts with lines 1-16, input IV-8, output I-1, etc. If the executive services less than four channels, Table 20 must be modified to delete references to those I/O slots that are not serviced.

Outputtable lines are connected to the real world only when the user installs an output module that is properly indexed. Inputs and outputs are used only in groups of 16 as required. They do not have to be indexed in consecutive order. Tables 7 and 10 define the allocated inputs and outputs for the possible I/O configurations established by the various executives.

The general servicing scheme of line solving, inputting, and then outputting data is then followed until either lines or inputs/ outputs are all serviced. At this time only the remaining category is serviced; thus the synchronization of input/output servicing versus line solving is maintained. Each I/O module is serviced individually with all 16 bits obtained from or provided to the module effectively in parallel, i.e., all at the same instant.

NOTE

If isolated I/O modules are utilized, 8 bits of information are obtained from each module (16 bits from each pair of modules).

When servicing input modules, the Processor requests the status of its 16 circuits twice and compares the two samples. If they agree, the data is stored in the I/O status; if they do not agree, another complete sample is requested and compared to the previously obtained status. This sampling is continued until two consecutive samples agree or until five compares are made. If, after five compares, no two consecutive samples agree, the Processor assumes all inputs are OFF (zero) for that input module and continues to scan. At the input module, if communications from the Processor are not received within 250 ms, the module will turn its active light OFF.

Output modules are provided with new status (all 16 outputs) at least twice each servicing; both transmissions are echoed to the Processor by the output module. The output module compares both sets of received data and, if they agree, uses them to drive its outputs. If they do not agree, the Processor re-transmits the data and a new compare is accomplished by the module between the most-recently received previous data and the new transmission; the re-transmission is initiated by the Processor's compare of the echoed data which will also be faulty. Up to four re-transmissions are accomplished if the echoes do not agree with the transmitted data. If, after a total of five comparisons, a valid compare is not obtained, the outputs retain their previous states and the Processor continues scanning. If the output module does not receive valid data within 250 ms, it will turn its active light OFF and shut all outputs OFF.

An attempt is made to communicate with each I/O module every scan regardless of the previous scan's results. Note that error checking is accomplished individually on all 16 bits provided or obtained from the I/O module. It is not a parity or error code verification.

4.1.3 Data Base

Data Base Description

The data base is composed of sequential words in the Controller memory that contain the information necessary to implement the control functions chosen by the designer for the logic lines of his system. For each logic line, exactly three 16-bit data words exist in the data base. The general format of the three words is as shown in Figure 107.

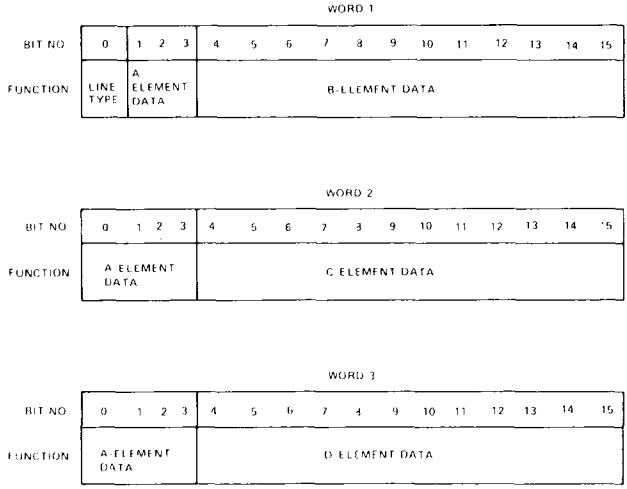


Figure 107. General Format of Logic Lines Data Base

The data base is accessed by the logic solver section of the Controller as the line is solved in the scanning process. For each logic line, three associated words are read out of the data base and interpreted.

If the logic line being interrogated is a relay line, the logic solver provides the solution. If the logic line is a non-relay function, the necessary data is passed to the software section of the Controller for the line solution. The logic solver determines the type of line by examining the line type bit (word 1, bit 0 of Figure 107). If the line is not a relay line, two additional bits in the third word are used to further classify the line as one of four other types. In this manner, the logic line is thereby classified as either a relay, counter, timer, calculate, or data transfer line.

The arrangement of data within the A, B, C, and D elements is dependent on the line type. For example, if relay contacts are associated with the A element, the data consists of the contact type and the address where the state of the reference controlling the contact is stored. In the case of a counter line, the element associated with the preset count would contain the constant (if the preset is fixed) or the address of the register that holds the desired preset count (if remote preset is utilized).

The exact contents of the words in the data base are established by the designer when he programs the Controller via the Programming Panel. An external computer can also be used to examine or alter the data base. In this case, the following descriptions provide the information required for interpretation of the codes. The beginning memory address of the data base is variable and dependent on the executive program used by a particular Controller; the specific allocation of core memory within the Controller for any individual MOPS/TEF can be obtained from the Service Center.

Data Base Formats

Detailed word format descriptions are provided in this section for the five types of logic lines that can be programmed: relay, counter, timer, calculate, transfer data. Three types of operands — discrete references, register references, and constants — are used in the data base. Discrete and register references are explained in the following paragraphs and are detailed in the word format descriptions.

Discrete References. Discrete references are addresses of individual data bits within the logic solver RAM (Random Access Memory). The logic solver RAM consists of sixty-four 16-bit words. The relative RAM address refers to a bit location in the RAM as shown in Figure 108.

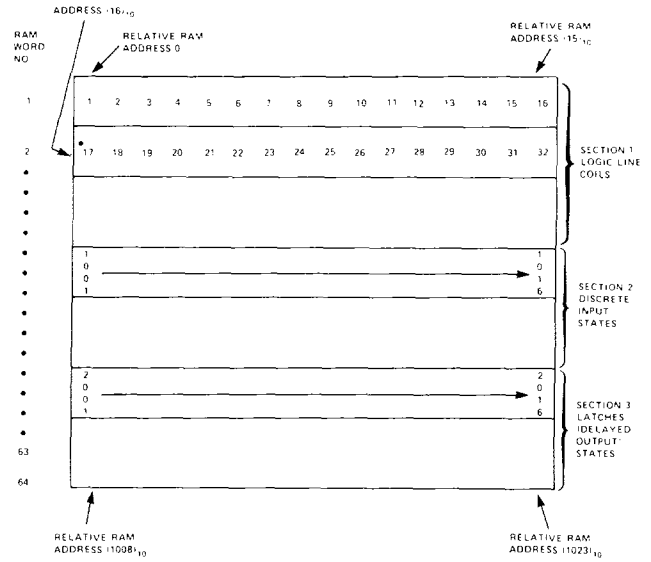


Figure 108. RAM Definition

To associate a relative RAM address with a line number, the configuration of a particular Controller and the three sections of the RAM must be considered. The size of section 1 of the RAM (in core words) consists of the number of Controller logic lines divided by 16. Each bit in a word indicates the state (coil) of one line; for example, bit 0 of word 1 is the state of logic line 0001, bit 1 in word 1 indicates the state of logic line 0002, etc. The state of these bits is controlled by the logic solver and the Controller hardware.

Section 2 of the RAM contains the states of the discrete inputs to the Controller whose address is determined by the Controller's executive. In order to associate a relative RAM address with a discrete input, the size of section 1 must be considered. Section 1 size is determined by the number of logic lines involved, as previously described. Similarly, section 2 consists of the Controller discrete inputs divided by 16 words. For example, consider a Controller with logic lines 0001 through 0224 and discrete inputs 1001 through 1224.

Section 1

Logic Line		Relative Address	
0001 — 1	=	0000	First logic line relative RAM address (bit 0 of word 1).
0002 — 1	=	0001	Second logic line relative RAM address (bit 1 of word 1).
↓		↓	
0224 — 1	=	0223	Last logic line relative RAM address (bit 15 of word 14; i.e., 224/16 = 14).

Section 2

L = Last logic line relative RAM address (e.g., 223).

Discrete Input		Relative Address	
L + 1	=	224	First discrete input (1001) relative RAM address (bit 0 of word 15).
L + 2	=	225	Second discrete input (1002) relative RAM address (bit 1 of word 15).
↓		↓	
L + 224	=	447	Last discrete input (1224) relative RAM address (bit 15 of word 28; i.e., 14 + 224/16 = 28).

For the example above, valid discrete input relative RAM addresses would fall in the range from 224 through 447.

Section 3 of the RAM contains the states of the latches (delayed outputs) of the Controller. To associate a relative RAM address with a latch, the size of sections 1 and 2 must be considered. To illustrate this, assume a Controller with latch 2001 through 2224 and the logic lines and discrete inputs as previously described. As stated, the last discrete input relative RAM address is 447.

Section 3

K = Last discrete input relative RAM address (e.g., 447).

Latch Number		Relative Address	
K + 1	=	448	First latch (2001) relative RAM address (bit 0 of word 29).
K + 2	=	449	Second latch (2002) relative RAM address (bit 1 of word 29).
↓		↓	
K + 224	=	671	Last latch (2224) relative RAM address (bit 15 of word 42; i.e., 28 + 224/16 = 42).

For the above example, valid latch relative RAM addresses are from 448 to 671.

NOTE

Since the logic solver RAM is always 64 words long, the number of lines, plus the number of discrete inputs, plus the number of latches, must be equal to or less than 1024.

Register References. Register references are addresses of words in the register table. The register table is a section of memory designated for input and holding register data. The words in the register table are referenced by the relative register address as shown in Figure 109.

In order to associate a relative register address with a specific input or holding register, the number of input registers for a particular executive program must be considered. For example, consider a Controller with input registers 3001 through 3016:

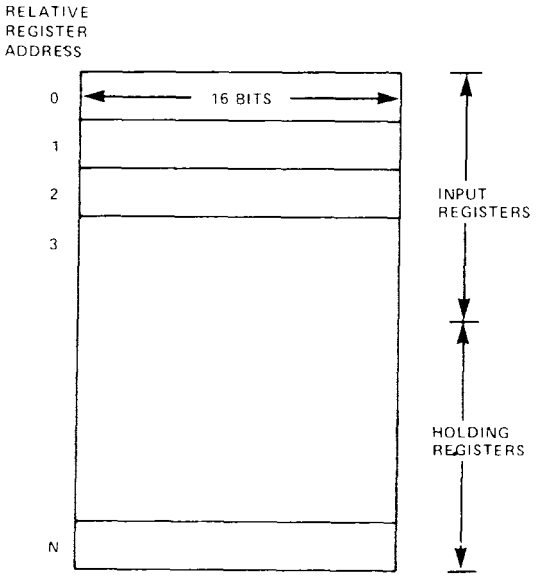


Figure 109. Definition of Register Table.

Input Register	Relative Register Address
3001	00
3002	01
↓	↓
3016	15

Holding register data is placed in the table beginning in the next location following the input registers. For the above example, where 15_{10} is the last input register, the holding registers would have relative addresses as follows:

Holding Register	Relative Register Address
4001	16
4002	17
↓	↓
4XXX	N

In the above example, N is the last relative register address that is required and is associated with the last holding register, 4XXX.

NOTE

Many executives provide more relative register address for input registers than are used by the standard I/O configuration. Consult the MODICON Service Center for specifics on any executive. These additional input registers can be utilized by I/O Allocation Table changes (typical maximum 32 register input) or to receive data from a monitoring computer.

For Controller configurations with no input registers, the holding registers are moved to the top of the table. Register 4001 would then have relative register address 00.

Word Formats. The five types of word format — relay, counter, timer, calculate, and data transfer — are designated by line type fields contained in data words 1 and 3 as shown in the following table.

	Word 1, Bit 0	Word 3, Bit 4	Word 3, Bit 5
Relay	0	—	—
Counter	1	0	1
Timer	1	1	0
Calculate	1	0	0
Data Transfer	1	1	1

The five types of formats are illustrated in the word format diagrams which follow (Figures 110, 111, 112, 113, and 114). The associated descriptions detail the data content of each word.

NOTE

The discrete and register references entered by the Programming Panel are automatically converted to relative references prior to their entry into core memory of the Controller.

NOTE

Since ten bits are available on the following diagrams for relative references (both discretes and registers), the number of unique discrete references must be equal to or less than 1024. In addition, the number of unique register references (input and holding) must also be equal to or less than 1024. These are separate limitations; both discrete and register references must be evaluated separately, and both must meet their limitation.

4.1.4 I/O Allocation Table

Table Description

The MODICON 184/384 Controller internally operates based on binary data. Normally, data received from the Programming Panel or input registers is converted from BCD to binary, and data provided to the Programming Panel or output registers is similarly converted from binary to BCD.

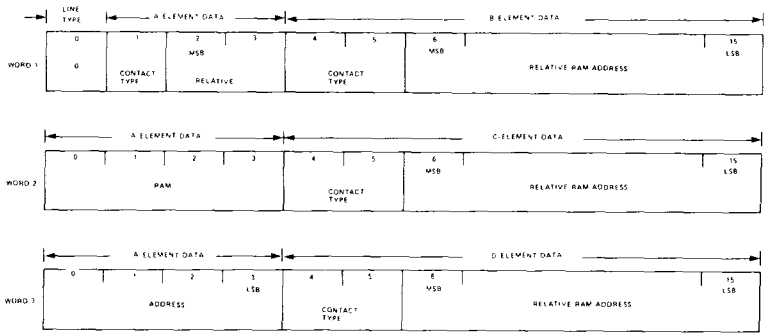
The Input/Output Control System software provides control of the sequence of I/O exchanges (transfers). The hardware ensures the sequences will start with channel I slot 1, and continue numerically to channel IV slot 8. The I/O allocation controls how the data obtained from or provided to the I/O modules is interpreted. *Any* I/O module can be coded for discrete or register data. Register inputs can be selected to be stored "as is" or converted from BCD to binary; register outputs also have the option to be converted from binary to BCD or outputted without conversion (binary outputs). In addition, particular input and output transfer can be inhibited without affecting the remaining I/O exchanges.

The interpretation of I/O exchanges is established by the I/O Allocation Table which is a directory of the relative logic solver RAM and register table addresses (see Figures 108 an 109). This table (see Figure 115) consists of thirty-two 16-bit words in the executive initially programmed by MODICON. Each word controls an I/O exchange to a particular I/O slot number. Bits 0 through 7 of each word control the input transfer while bits 8 through 15 control the output transfer.

NOTE

Because of its functions, the I/O Allocation Table is commonly referred to as the "Traffic Cop."

RELAY LINE



LINE TYPE

Word 1	Bit 0	0	Indicates Relay Line

A ELEMENT DATA

			Contact Type
Word 1	Bit 1	0	Series Normally Open
		1	Series Normally Closed
Word 1	Bit 2	MSB	Relative RAM Address
	Bit 3		
Word 2	Bit 0		
	Bit 1		
	Bit 2		
	Bit 3		
Word 3	Bit 0		
	Bit 1		
	Bit 2		
	Bit 3	LSB	

B, C, D ELEMENT DATA

	Contact Type
0 0	Series Normally Open
0 1	Series Normally Closed
1 0	Parallel Normally Open
1 1	Parallel Normally Closed

Relative RAM Address

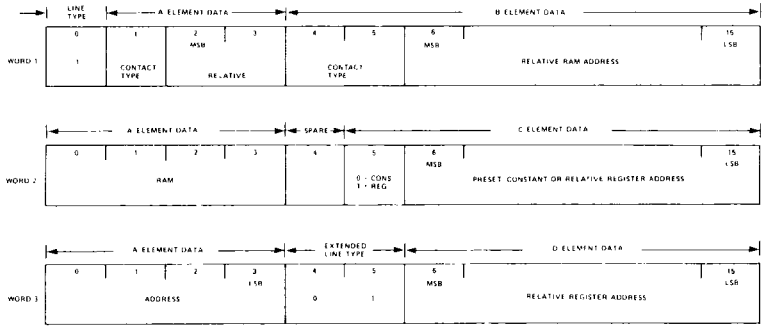
Bit 0 — MSB

Bit 15 — LSB

NOTE: MSB = most-significant bit
LSB = least-significant bit

Figure 110. Relay Line Word Format

COUNTER LINE



LINE TYPE

Word 1 Bit 0 = 1
Word 2 Bit 4 = 0 — Indicates Counter Line
Word 3 Bit 5 = 1

A ELEMENT DATA

			Contact Type
Word 1	Bit 1	0	Series Normally Open
		1	Series Normally Closed
Word 1	Bit 2	MSB	Relative RAM Address
	Bit 3		
Word 2	Bit 0		
	Bit 1		
	Bit 2		
	Bit 3		
Word 3	Bit 0		
	Bit 1		
	Bit 2		
	Bit 3	LSB	

B ELEMENT DATA

	Contact Type
0 0	Series Normally Open
0 1	Series Normally Closed
1 0	Parallel Normally Open
1 1	Parallel Normally Closed

Relative RAM Address

Bit 6 (MSB) ↓ Bit 15 (LSB)

C ELEMENT DATA

Constant/Register (Bit 5)

0 — Indicates the data in bits 6 through 15 is a constant

1 — Indicates the data in bits 6 through 15 is a relative register address

Preset (Bits 6 through 15)

Bit 6 (MSB) ↓ Bit 15 (LSB) — Constant = binary equivalent of 0 to 999. Indicates desired count

Register Address = indicates desired register (1-8) contains the desired count (Remote Preset)

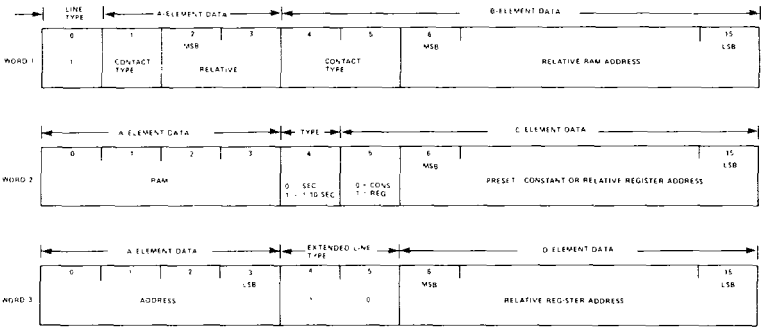
D ELEMENT DATA

Relative Register Address

Bit 6 (MSB) ↓ Bit 15 (LSB) — Indicates the register in which the accumulated count is to be stored

Figure 111. Counter Line Word Format

TIMER LINE



LINE TYPE

Word 1 Bit 0 = 1
Word 3 Bit 4 = 1 Identifies Timer Line
Word 3 Bit 5 = 0

A ELEMENT DATA

Contact Type

Word 1 Bit 1: 0 Series Normally Open; 1 Series Normally Closed

Word 1 Bit 2 (MSB) through Word 3 Bit 5 (LSB): Relative RAM Address

B ELEMENT DATA

Contact Type

0 0 Series Normally Open
0 1 Series Normally Closed
1 0 Parallel Normally Open
1 1 Parallel Normally Closed

Relative RAM Address

Bit 6 (MSB) through Bit 15 (LSB)

TYPE

Timer Resolution (Bit 4)

0 Indicates data defined by bits 6 through 15 is in seconds

1 Indicates data defined by bits 6 through 15 is in tenths of seconds

C ELEMENT DATA

Constant/Register (Bit 5)

0 Indicates data in bits 6 through 15 is a constant

1 Indicates data in bits 6 through 15 is a relative register address

Preset (Bits 6 through 15)

Bit 6 (MSB) through Bit 15 (LSB):
Constant = binary equivalent of 0 to 999. Indicates desired time in seconds if bit 4 is 0, or 1/10 seconds if bit 4 is 1.
Register Address = indicates designated register contains desired time, expressed in seconds if bit 4 is 0, or 1/10 seconds if bit 4 is 1.

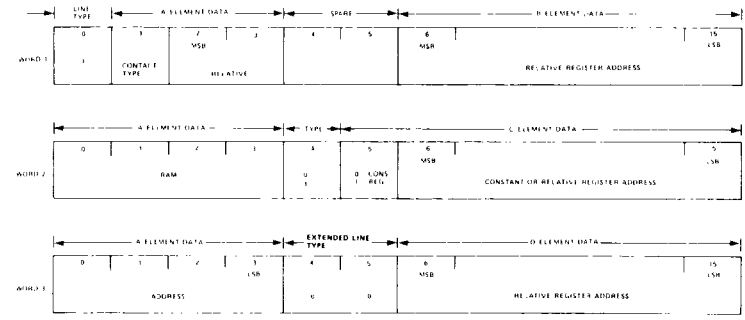
D ELEMENT DATA

Relative Register Address

Bit 6 (MSB) through Bit 15 (LSB): Indicates the register in which elapsed time is to be stored either in seconds if bit 4 word 2 is 0, or in 1/10 seconds if bit 4 word 2 is a 1.

Figure 112. Timer Line Word Format

CALCULATE LINE



LINE TYPE

Word 1 Bit 0 } 1
Word 3 Bit 4 } 0 Identifies Calculate Line
Word 3 Bit 5 } 0

A ELEMENT TYPE

Contact Type

Word 1 Bit 1 — 0 Series Normally Open
1 Series Normally Closed

Word 1 Bit 2 — MSB
Bit 3
Word 2 Bit 0
Bit 1
Bit 2
Bit 3
Word 3 Bit 0
Bit 1
Bit 2
Bit 3 — LSB
} Relative RAM Address

B ELEMENT DATA

Relative Register Address

Bit 6 — MSB
Bit 15 — LSB
} Indicates register in which B portion of calculation is stored

TYPE

Add or Subtract (Bit 4)

0 Indicates the calculation is B + C
1 Indicates the calculation is B − C

C ELEMENT DATA

Constant/Register (Bit 5)

0 Indicates data in bits 6 through 15 is a constant
1 Indicates data in bits 6 through 15 is a relative register address

Bits 6 through 15

Bit 6 — MSB
Bit 15 — LSB
} Constant — binary equivalent of 0 to 999. Value of C portion of B + C calculation if bit 5 is 0.
Register Address — indicates designated register contains C portion of B + C calculation, if bit 5 is 1.

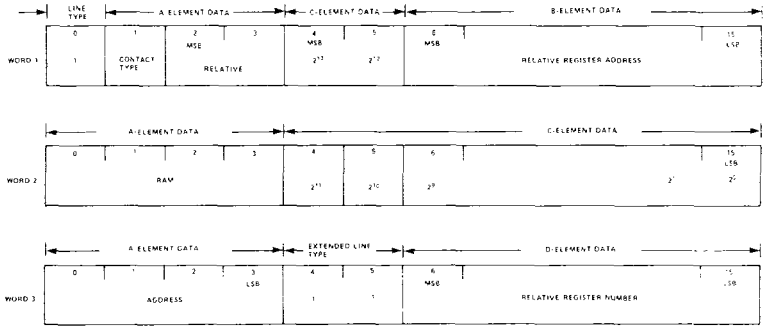
D ELEMENT DATA

Relative Register Address

Bit 6 — MSB
Bit 15 — LSB
} Indicates register in which results of B + C calculation is to be stored

Figure 113. Calculate Line Word Format

DX LINE



LINE TYPE

Word 1 Bit 0 } 1
Word 3 Bit 4 } 1 Identifies Data Transfer Line
Bit 5 1

A ELEMENT DATA

Contact Type

Word 1 Bit 1 0 Series Normally Open
1 Series Normally Closed

Word 1 Bit 2 MSB
Bit 3
Word 2 Bit 0
Bit 1
Bit 2
Bit 3
Word 3 Bit 0
Bit 1
Bit 2
Bit 3 LSB
} Relative RAM Address

B ELEMENT DATA

Relative Register Address

Bit 6 MSB
Bit 15 LSB
} Indicates designated register that contains data to be acted on

C ELEMENT DATA

Word 1 Bit 4 MSB
Bit 5
Word 2 Bit 4
Bit 15 LSB
} Function Call: Binary equivalent of four digit base 10 number
Format of the function call is shown below

X X X X
Function Call Identifier — Function Call Modifier

Function Call Identifier: Code to designate the operation to be performed. Examples of the code are:

1XXX Move
2XXX Matrix
3XXX Extended Arithmetic
4XXX Print

Function Call Modifier: Code to elaborate upon the function call. Examples are:

1XXX

210 Move data from a single register into a table 10 registers long every time A contact closes
534 Load a 34-register FIFO (First In First Out) stack

2XXX

005 Logical AND between two matrices each five registers long (80 bits)
212 Matrix compare each scan of two matrices each 12 registers long (192 bits)

3XXX

000 Multiply
100 Divide
400 PID

4XXX

001 Print contents of one register
125 Print form message number 25

D ELEMENT REGISTER

Relative Register Address

Bit 6 MSB
Bit 15 LSB
} Indicates designated register where results of transfer are to be placed

Figure 114. Data Transfer Line Word Format

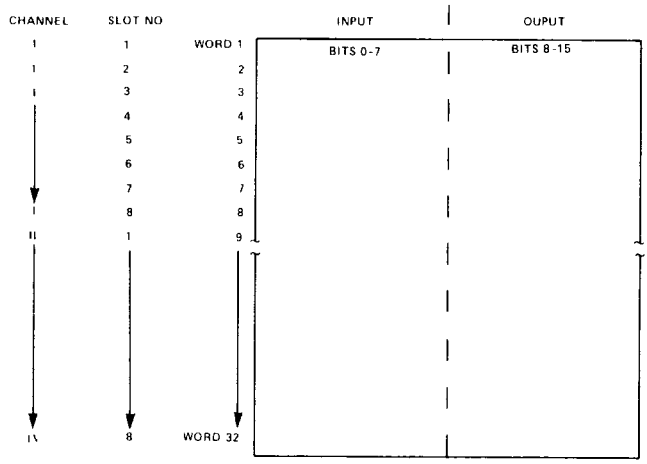


Figure 115. Word Definition in I/O Allocation Table

At the end of each group of 16 line solutions, the I/O control system initiates a transfer. Both the logic solver line solutions and the I/O Allocation Table are sequenced by the same index. The table is sequenced starting at word 1, and for one complete sweep of the executive program all I/O transfers in the table are performed. The desired results of I/O transfers can be obtained by assigning an I/O module to the appropriate location within the I/O structure.

Each word in the I/O table contains a 5-bit input-relative address and a 5-bit output-relative address to direct the I/O data to or from the appropriate memory location (refer to Figure 116). Each input or output group consists of 16 lines of discrete data or 16 bits of register data. Bits are set in the input and output control field of the I/O Allocation Table word to indicate whether the transfer is discrete data or register data and, if register data, is it binary (no conversion) or BCD (conversion to binary required).

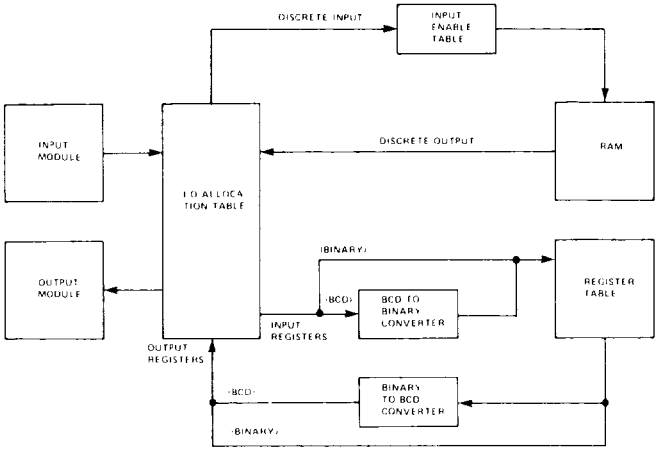


Figure 116. Block Diagram of I/O Transfers

The 16 bits of discrete input are directed by the I/O Allocation Table input-relative address to the assigned storage location within the logic solver RAM. The input is routed to the logic solver RAM through the Input Enable table. Data in the Input Enable table can inhibit transfer of selected discrete inputs if the disable feature has been utilized.

When a discrete output transfer is indicated by the I/O Allocation Table word control field, the relative output address controls where in the logic solver RAM the data is obtained, and directs it to the appropriate output module.

The 16 bits of register input data are directed by the I/O Allocation Table input-relative address to a specified position within the register table. Register input data can either be BCD or binary. If the register data is to be stored "as is" (e.g., already is binary), the I/O Allocation Table routes the input data directly to the register table. However, if the data is BCD, it must be converted to binary prior to being placed in the register table. This is done by setting a bit in the I/O Allocation Table word input control field.

Register output data can also be transferred "as is" to the output module or converted to BCD as controlled by a control bit in the I/O Allocation Table word.

Word Format

The word format for the I/O Allocation Table and a description of the format by field and bit assignments is provided in Figure 117. In addition, an explanation of the relationship of the relative input and output address with respect to memory location within the RAM and register table is provided in the following paragraphs.

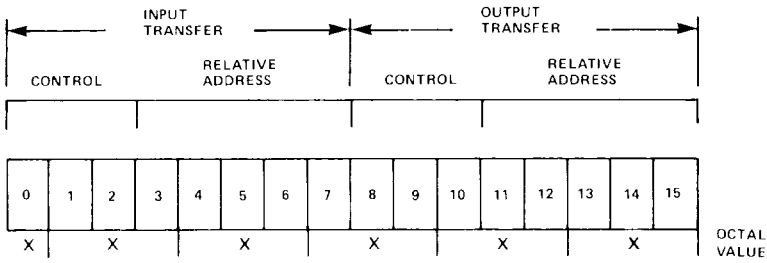
Discrete Data Addresses. The logic solver RAM consists of sixty-four 16-bit words divided into three sections. Section 1 contains the state of line solutions (outputs); section 2 contains the state of the discrete inputs to the Controller; and section 3 contains the latches (delayed outputs). Latches are not addressable by the I/O Allocation Table.

A relative input address selects the appropriate word within section 2 of the logic solver RAM to store the 16 discrete inputs. In section 2, the discrete inputs are stored in numerical sequence as follows: relative input 00 selects discrete inputs 1001 through 1016, relative input address 01 selects discrete inputs 1017 through 1032, etc. The maximum discrete input-relative address is calculated by dividing the number of discrete inputs by 16.

A relative output address selects the appropriate word (16 bits) within section 1 for loading as coil outputs to an output module. In section 1, the coil outputs are stored in numerical sequence starting at word 1 (relative address 00) as follows: relative output 00 selects coil output lines 0001 through 0016, address 01 selects coil outputs 0017 through 0032, etc. The maximum coil output-relative address is calculated by dividing the number of logic lines by 16 not to exceed 32.

Since the I/O Allocation Table provides five bits for relative addressing, the system could load 32 words into the RAM from discrete inputs (maximum 512 discrete inputs) and output 32 words from the RAM for coil outputs (maximum 512 discrete outputs). Such a system would have 512 logic lines and no latches since the RAM is 64 words long. Changes to the I/O Allocation Table cannot be made to provide more discrete outputs than logic lines, nor more discrete inputs than established by the particular executive. The maximum relative addressing (32) is the same as the total number of I/O slots provided with the Controller (8 X 4 = 32).

Register Data Addresses. Relative register input and output addresses are locations in the register table. The register table is a section in memory designated for input and holding register data. The length of the table is determined by the number of input registers plus the number of holding



INPUT CONTROL

Bit 0 Input Word Transfer Inhibit
- 1 Disable: Indicates input data transfer for this input slot not to be performed.
- 0 Enable: Indicates input data transfer for this input slot to be performed.

Bit 1 Discrete Register Identifier
- 1 Register: Indicates input relative address is a register table address.
- 0 Discrete: Indicates input relative address is a logic solver RAM word address.

Bit 2 Register Data Type
- 1 - BCD: Indicates register data is to be converted to binary prior to storing in register table.
- 0 - Binary: Indicates register data is to be stored "as is" in register table.

INPUT RELATIVE ADDRESS

Bits 3-7 Relative Address 0 through 37_8:
Indicates relative RAM word or input register address as determined by the setting of bit 1.

OUTPUT CONTROL

Bit 8 Output Word Transfer Inhibit
- 1 Disable: Indicates output data transfer for this output slot not to be performed.
- 0 Enable: Indicates output data transfer for this output slot to be performed.

Bit 9 Discrete Register Identifier
- 1 Register: Indicates output relative address is a register table address.
- 0 Discrete: Indicates output relative address is a logic solver RAM word address.

Bit 10 Register Data Type
- 1 BCD: Indicates data stored in register table is to be converted to BCD before output transfer.
- 0 Binary: Indicates data stored in register table is to be transferred "as is".

OUTPUT RELATIVE ADDRESS

Bits 11-15 Relative Address 0 through 37_8:
Indicates relative logic solver RAM word or output register table address as determined by setting of bit 9.

Figure 117. Word Format in I/O Allocation Table.

registers for a particular executive program. The first entry in the table, relative input address 00, is input register 3001; the second is 3002, etc. Thus, if an executive program has input register 3001 through 3016, the corresponding relative input addresses in the I/O Allocation Table are 00 through 15. A maximum of 32 input registers can be addressed by the I/O Allocation Table.

The holding registers follow the input registers. In the I/O Allocation Table, only the first 32 holding registers (4001 through 4032) in the register table can be transferred to output modules. For executive program configurations with no input registers, relative output address 00 through 32 would still denote holding registers 4001 through 4032. However, there is no executive currently written that provides only register outputs; whenever register I/O is available, both input and output registers are provided.

The maximum number of register I/O is normally greater than that provided with the basic executives as listed in Tables 11 and 12. Generally up to 32 input registers and 32 output registers, as a maximum, can be provided by altering the standard I/O Allocation Table; the exact limitations on maximum register I/O for each MOPS/TEF is available from the Service Center and should be verified prior to utilizing more than 16 input registers.

Modifications to I/O Allocation Table

Since the I/O Allation Table is part of the executive, changes to it can only be accomplished by a computer interface with the Controller's memory protect OFF. A unique I/O Allocation Table can be designed and loaded into the

Controller at time of shipment, or via a Telephone Interface and the Service Center. The major flexibility of this table allows the designer to make changes as to how the I/O is configured; however, if discrete and register modules are intermixed in the same channel, then identification of each module's function is mandatory in order to minimize maintenance procedures. Thus it is recommended that changes to the I/O Allocation Table be normally limited to reasons of necessity and not convenience. Some valid reasons for altering the standard table provided with the executive are as follows:

1. Make individual register I/O binary instead of BCD (Analog I/O).
2. Increase the number of register I/O (either input or output) at the expense of discretes.
3. Increase the number of discrete outputs (at the expense of register outputs).

NOTE

Changes to the I/O Allocation Table *cannot* be made that provide more discrete inputs than allowed by the executive.

4. Mixing discrete and register I/O in a channel that is to be remoted (i.e., driven from 1425 Remote Driver).
5. Output any of the first 32 holding registers (4001-4032) or first 512 line coils (in groups of 16) in lieu of standard discrete outputs without changing the total discrete vs register output mix.

4.1.5 Power-Up/Power-Down Sequence

When power is initially applied to the Main Power Supply (P420), it begins to generate dc power (±5 Vdc) required to operate the logic within the Processor and the I/O. As soon as both of these supplies are within tolerance (±0.5% on + 5 Vdc and ± 1.0% on −5 Vdc), a power OK signal is sent to the Processor. This power OK signal remains available until the power supply detects a loss of ac power, at which time it removes the power OK signal prior to loss of the ±5 Vdc power.

As soon as the power OK signal is received, the Processor goes through a special power-up sequence. This sequence takes approximately 500 milliseconds and includes clearing the logic solver RAM (see Figure 108), updating the latches with the retained coil status, scanning inputs and updating status (discrete inputs plus input registers), then beginning scanning the logic at line 1.

As part of the power-up sequence, all DX printer lines will be cleared (coil OFF) and lines representing print commands awaiting servicing will be cleared (removed from queue). The A element history table, that represents previous status of discrete references for use with counter and some DX lines, is not altered and retains its previous state.

When scanning begins at line 1, all subsequent line coils will be assumed to be OFF. As the lines are scanned and solved, their coil status will be provided to the RAM for immediate reference by all subsequent lines. The power-up sequence does not alter the status of any registers; their previous contents will be retained unless altered by the logic lines.

Whenever the power OK signal is removed, the Processor goes through a power-down sequence. It completes whatever instruction is currently being operated on; this ensures that data read from core memory is rewritten back into core. Data cannot be lost even if power is shut down during a core read/write operation. The scanning is terminated at whatever line is currently being executed; the Processor does not wait until the end of a scan to stop operation. All outputs are forced to zero (OFF condition) and the run light extinguished. Since the power OK signal is removed prior to actual loss of the dc power, there is sufficient time to ensure an orderly shutdown whenever ac power is removed.

4.2 SERVICE CENTER

4.2.1 Services

The Service Center is an office at MODICON's headquarters in Andover, Massachusetts that is manned 24 hours per day, 365 days a year. This office provides maintenance assistance to MODICON's customers at any time of the day or night. At the Service Center, there are several data telephone lines, support computers, and extensive files on all Controllers manufactured by MODICON. Any data line can be obtained by calling (617)475-1181. If one line is busy, the call is automatically transferred to the next available line. Since the center is always manned, this telephone number should be made available to maintenance personnel as the first option they exercise when assistance is required.

Figure 118. Telephone Interface

To make maximum use of the Service Center's capabilities, a Telephone Interface (Figure 118) should be available. This interface connects to the 184/384 Controller's Processor and allows the support computers to communicate directly to the Controller. Complete operating instructions for this interface are provided in Appendix A, Auxiliary Units. With the interface connected, the computer can:

1. Record the Controller's memory contents onto paper tape for storage at the Service Center.
2. Reload a Controller's memory from previously made paper tape.
3. Generate a ladder diagram of the user's logic, complete with cross-references and optional mnemonic identification.
4. Exercise a Controller with special diagnostic programs to locate hardware faults.
5. Load a Controller's memory with any executive available from MODICON.
6. Makes changes to the I/O Allocation Table (Traffic Cop) — see 4.1.4.

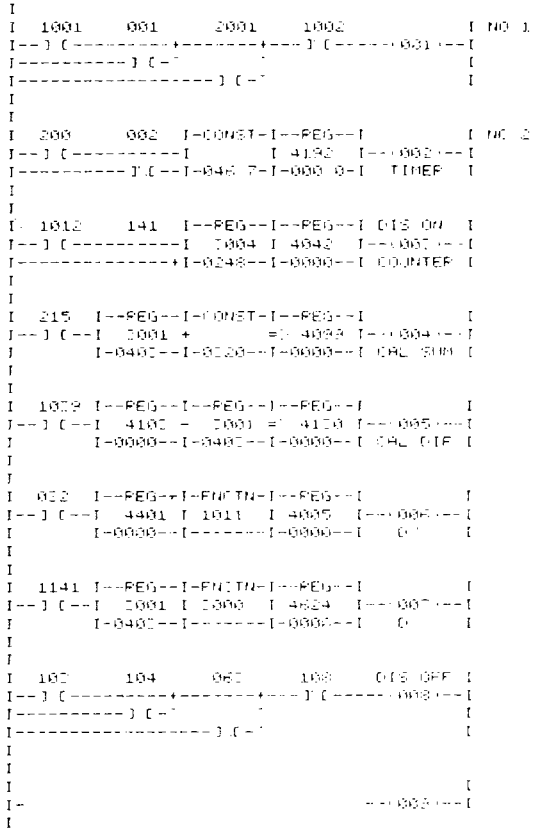


Figure 119. Typical Ladder Diagram Printout

When a Controller's memory content is to be recorded onto paper tape ("dump" into the Service Center), the entire core memory (executive, logic, register contents, and I/O status) is recorded. Thus, if a reload is required, due to operator error (e.g., power supply disconnected while the Controller is running, a wrong program loaded by magnetic tape, or unauthorized changes are made), or a duplicate machine is being programmed, or hardware malfunction, the entire core memory is restored to the status it held at the time of the "dump." Any I/O Allocation Table changes, stored register contents, disable status, etc. will be included in the reload.

Programs are stored by the Controller's serial number, located on the top, forward, right-hand corner of the Processor. This serial number should be referred to whenever the Service Center is contacted for assistance. Upon request, the Service Center can store more than one program under a serial number, provided clear identification is made between programs; or the program can be identified with a "tag" agreed upon between the user and the Service Center, thus allowing the serial number to be ignored.

Also stored by serial number, along with the latest core dump on paper tape, is the manufacturing history of the Controller, a summary of all previous service calls, notations of I/O Allocation Table changes, and identification of executive currently in the Controller. Thus, if a problem occurs

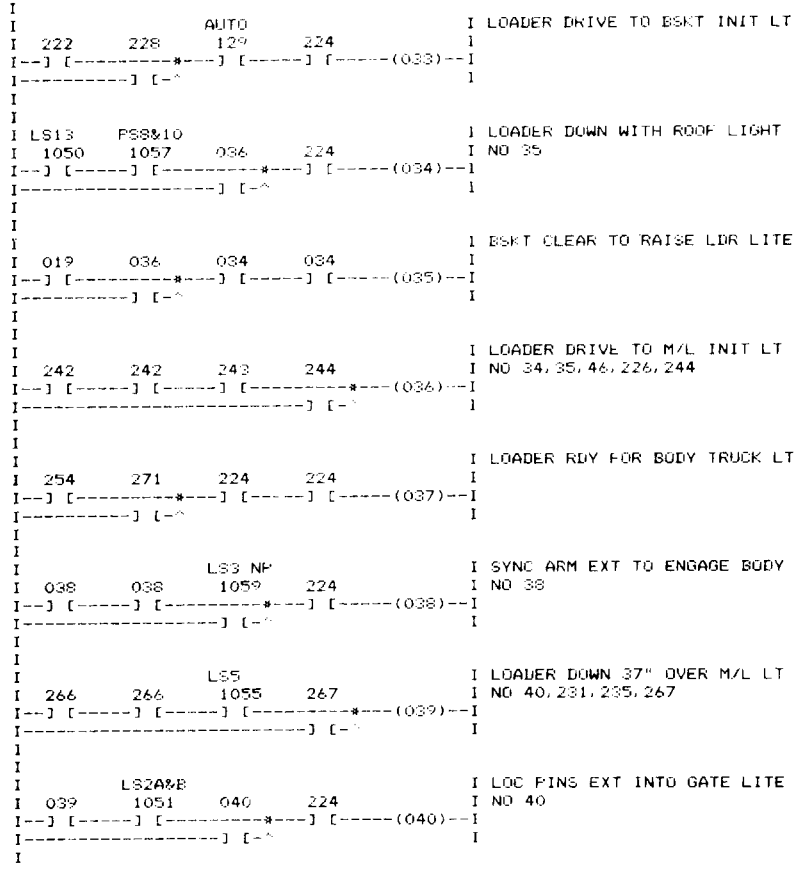


Figure 120. Ladder Diagram with Mnemonics

at 3:30 a.m., the Service Center operator can review previous communictions and determine if a change was made at 11:30 a.m. on the previous day that may have some effect on the problem. Diagnostic programs can also be used to exercise the Controller and locate areas of malfunction. In addition to maintenance support, the Service Center can reload executives (MOPS and TEF), make changes to the I/O Allocation Table, or determine which executive is in the Controller.

4.2.2 Ladder Diagram Documentation

Once the program is stored on paper tape, a ladder listing can be generated as illustrated in Figure 119. This listing documents the entire user's program utilizing the same reference numbers that were used to enter the program in all four elements of each logic line. An extensive cross-reference is also provided that indicates where each line coil is referred to in the logic, and whether the reference is to a normally-open or normally-closed contact. In addition, at the end of the listing, a cross-reference is provided indicating where all discrete inputs, latches, and registers (input, output, or holding) are used as well as the contents of *all* registers.

As an optional feature, mnemonic information can be added to each logic line and discrete input. This information can be used to label the logic lines as to where they are wired in the system if they are also discrete outputs, or to indicate the function of the logic line. The discrete inputs can also be labeled as to where they are connected in the system. Figure 120 has the optional mnemonic information added to it. Utilizing this option, documentation and troubleshooting of a control system is extremely simple.

Figure 121 provides a sample form that can be used to provide MODICON with your desired mnemonic information; additional forms are available on request from MODICON. Each logic line or input can be assigned a six-character name (e.g., LS37), which will appear in the ladder diagram above each and every contact referred to this logic line or input. A complete label, up to 28 characters, can be assigned to any and all logic lines; discrete inputs can be labeled with up to 53 characters. These complete labels will appear opposite the coil of the logic line and opposite the cross-reference of discrete inputs at the end of the ladder diagram.

4.2.3 System Maintenance Support

The above services assume a Telephone Interface is available. If this unit is not available at the time the Service Center is contacted, some limited assistance can still be provided. Assuming all or a portion of the control system is malfunctioning, step-by-step maintenance instructions can be provided and the responses analyzed. A typical discussion could be:

Customer (C) *Service Center Operator (O)*

C: My system is down.

O: What type of Controller do you have?

C: I do not know; it's big.

O: Do you know where the Processor is?

C: Yes.

O: What does it look like, just the Processor

C: It is square, about 18 in. long, 12 in. high, and 12 in. deep, gold in color.

O: On the top of the Processor, is there a tag marked 184?

C: Yes.

O: After the 184, what is the dash number?

C: Two.

O: On the top right corner, there is a silver tag. What is the serial number on that tag?

C: 1313.

O: You have a 184 Controller, serial number 1313 with 2K memory. Is your entire control system down?

C: Yes.

O: Above the Processorn generally to the left, is a power supply. Are both lights on the top of this power supply ON?

C: Yes.

O: At the bottom of the power supply, there are two lights; are they both ON?

C: Yes.

O: On the Processor, below the large black knob on the front are five lights. Is the top one ON?

C: Yes.

O: Are any other lights ON?

MODICON

LADDER DIAGRAM NAME & COMMENT FORM

ENGINEER _____ MODICON SERIAL NUMBER _____

DIAGRAM NAME _____ DATE _____

NUMBER LETTER CONVENTION 0 ZERO O LETTER O OR 1 ONE
I LETTER I 2 TWO Z LETTER Z

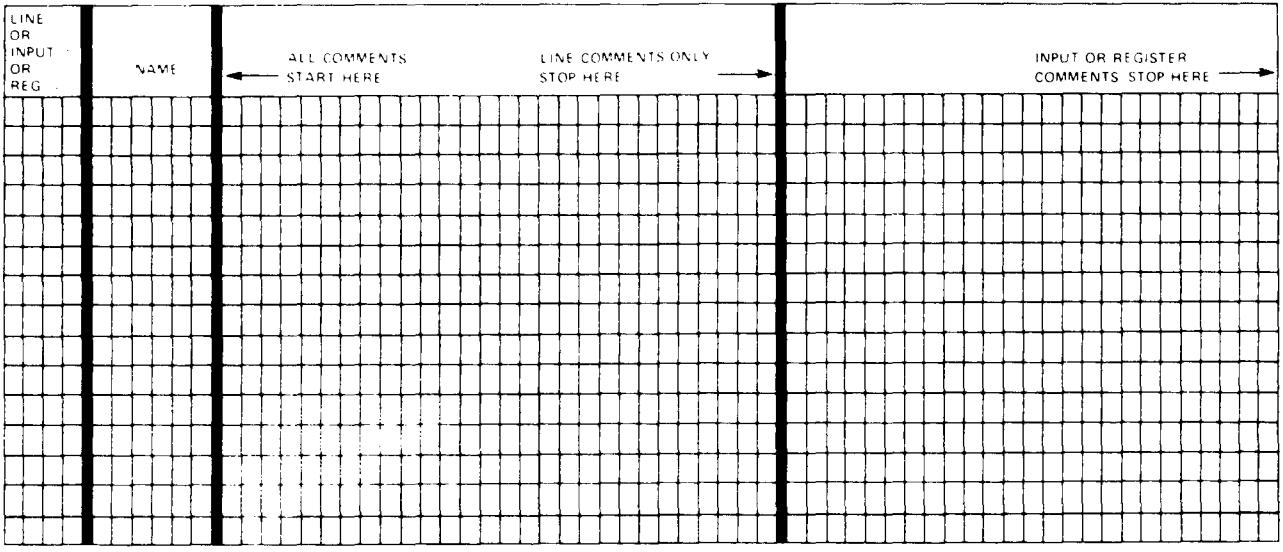


Figure 121. Form for Specifying Mnemonics

C: Yes, the first three are blinking; the last one is OFF.

O: On the bottom of the Processor, below these lights, are three receptacles. How many have large black cables connected.?

C: All three.

O: Follow the large black cable connected to the last receptacle, the one closest to the mounting plate. Where does it go?

C: It goes to a large box.

O: What does this box look like?

C: It is about 24 in. tall, 12 in. deep, and 8 in. wide, gold in color, and is connected to other things.

O: That appears to be an auxiliary power supply. At the top should be three wires coming in and some jumpers. Is the light on the top ON?

C: No.

O: It appears that there is no ac power to this auxiliary power supply. Can you check this out with a meter and determine the problem?

C: Yes.

O: Please call me back if restoring ac power does not correct your problem.

If a ladder listing of the program in the Controller has been made, a carbon copy is kept at the Service Center again under the Controller's serial number. When a control system (not just the Controller) malfunctions, the Service Center operator can "walk" the maintenance technician through this logic with the Programming Panel and assist him to determine the cause of the fault. This cause may be a failed limitswitch, solenoid, relay, etc., or could be a failed I/O module or Processor. Whatever the cause, the Service Center is interested in solving your problems, whatever they are, at any time day or night, without having to obtain the services (3:30 a.m.!!) of the control engineers or maintenance supervisors. However, assistance provided can only be as reliable as the data previously provided to the Service Center. If changes are made to the program after a "dump" has been made, they should be clearly documented or another "dump" made into the Service Center to update its data.

4.3 COMMUNICATIONS WITH A COMPUTER

Introduction

As an option, the 184/384 Controller can be equipped with a Computer interface (Figure 122). This interface provides an EIA specification number RS-232C (Type E) data port to the Controller; RS-232C interfaces are recognized industrial standards. The hardware considerations of this Computer Interface (I646) are discussed in Appendix A. This section describes the operations and software considerations required to provide reliable communications to a computer.

The computer must be equipped with RS-232C matching data port, normally a standard hardware option with most computer manufacturers. The MODICON Computer Interface standard baud rates are: 300, 2400, 4800, and 9600; optional rates on special order are: 150, 200, 600, 900, 1200, 1800, 3600, and 7200. Once installed, the interface can provide the computer with full access to the Controller's core memory. Only one computer can be connected via the Computer Interface to the Controller at a time; however, the Controller can communicate to both a computer and the Programming Panel at the same time.

RS-232C Details of Operation

The RS-232C interface is an asynchronous, full-duplex, serial communication device. Figure 123 illustrates the basic format of this serial transmission. Each character is defined as eleven bits; one start bit, eight

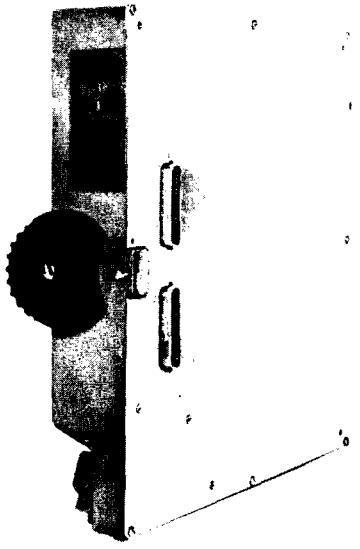


Figure 122. Computer Interface.

data bits, and two stop bits. As soon as one character has been sent, a sec ond and subsequent characters can follow immediately in serial format there is no requirement to delay between character transmission. The length of time to transmit a character depends on the baud rate of the Com puter Interface. Table 21 summarizes the minimum time to transmit a character and a single bit for the available baud rates. Since the 184/384 Controller is a 16-bit machine, it requires two RS-232C character transmis sions to convey the information in one word of the Controller's memory (see Figure 124). The least-significant bit is the first bit to be transmitted.

NOTE

The computer interface will operate with either one or two (or more) stop bits; it echos back whatever format it receives. Two stop bits will be utilized for illustrative purposes here.

Table 21. Minimum Times for Single Character or Bit Transmissions

BAUD RATE (Bits per Second)	One RS-232C Character	TIME (ms) REQUIRED FOR: One Bit
150	73.3	6.67
200	55.0	5.00
300	36.7	3.33
600	18.3	1.67
900	12.2	1.11
1200	9.2	0.83
1800	6.1	0.5
2400	4.6	0.42
3600	3.0	0.28
4800	2.3	0.21
7200	1.5	0.14
9600	1.1	0.10

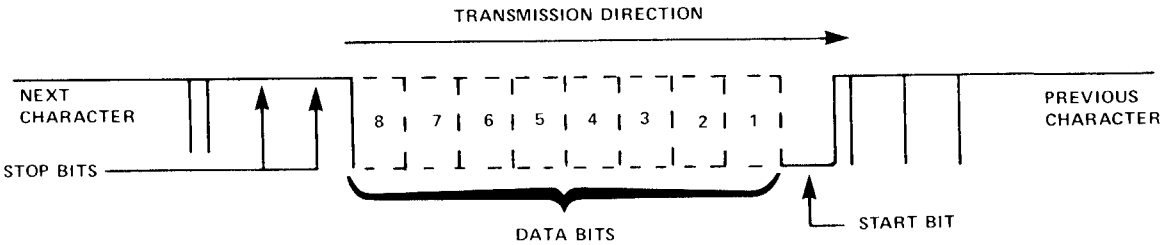


Figure 123. Format of RS-232C Serial Transmission

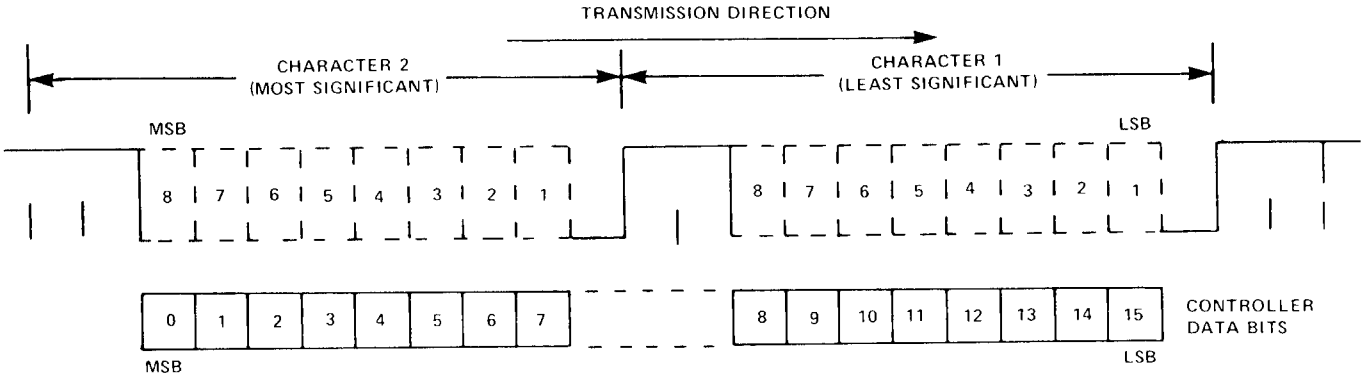


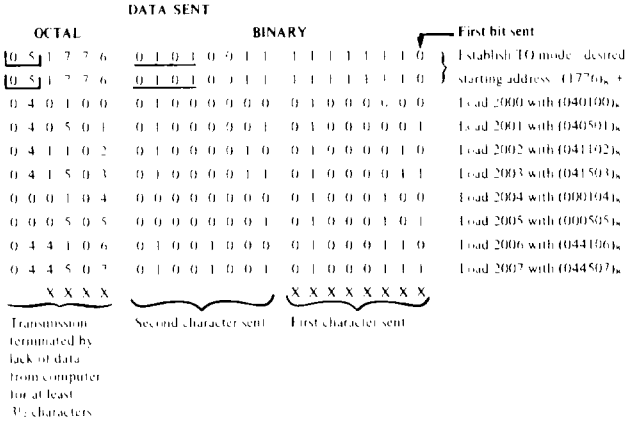
Figure 124. Format of Controller's 16-Bit Word Transmission

Communications

When power is first applied to the Computer Interface, it will assume the idle state. In order to activate the interface, the computer must provide, to the interface, a special code that establishes the mode of operation, either "TO" or "FROM" the CONTROLLER. This special code includes the core address in the Controller where the transmission is to start; transmissions continue from that address each time being automatically incremented by one (e.g., 0160, 0161, 0162, etc.) until the transmission is terminated by the computer. To terminate a transmission, the computer merely stops sending characters for the time normally required to transmit 3½ characters (3.9 ms minimum at 9600 baud). Once terminated, the transmission must be re-initiated with a special "TO" or "FROM" code. To provide error checking, whenever these special codes are utilized, the complete transmission (code and starting address) must be sent twice.

TO Mode

To establish a "TO" mode of operation, wherein data is to be sent to the Controller for storage in its core memory, the code 0101 is utilized. In addition to the code, the starting address *minus 2* must also be provided. Table 22 lists some example values of desired starting location and the actual value to be transmitted. Since the maximum core memory size in the 184/384 Controller is 4K (4096 words), 12 bits are required to address any core location. Thus, with four bits added for the special direction code, 16 data bits must be sent to establish a TO transmission starting at a particular core address. Each time these 16 bits are transmitted, they must be sent twice. Following these two transmissions (each of two 11-bit characters), the data to be placed in memory is provided (two 11-bit characters per word to be loaded). The following is an example of transmission into core location 2000-2007:



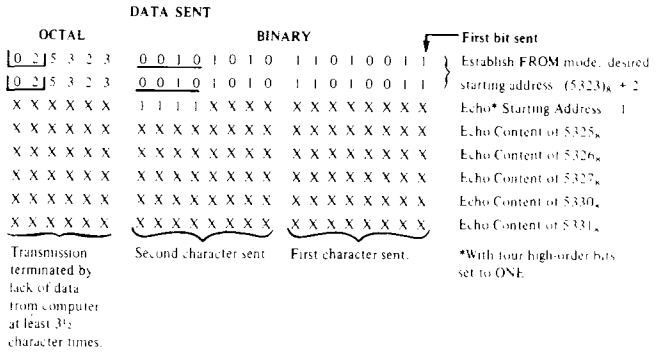
Each bit transmitted is echoed back to the computer for error checking via the duplexed communications. The bit will be sent back or echoed slightly delayed from its reception; this delay is one-half of the time it takes a bit to be transmitted (0.05 ms at 9600 baud). These bits can be compared by the computer to the data transmitted if the proper software is written, and any errors detected. This error checking is not accomplished using a parity or some other error checking code, but rather by an entire retransmission and complete compare. If an error is detected, the transmission can be terminated and re-started at an earlier error-free location. Data is actually loaded into the core memory after the next RS-232C character (11 bits) is received. Thus, on the previous example, one character of any eight data bits (represented by X's) is sent to force the last word received (044507) into location 2007 prior to terminating the transmission.

Table 22. Starting Addresses vs. Address Sent

Desired Starting Address (Octal)	Actual Value Transmitted (Octal)
0	7776
1	7777
2	0000
777	0775
1230	1226
2000	1776
2037	2035
3777	3775
5325	5323
7775	7773
7777	7775

FROM Mode

To establish a FROM mode of operation, wherein data is to be sent FROM the Controller, the code 0010 is utilized. Data is copied out of its core memory (non-destructive, retentive copying). In addition to the code, the starting address *minus 2* must also be provided (see Table 22). Again, a 16-bit transmission (4 bits for code, 12 bits for address) is sent to establish a FROM transmission and must be sent twice. These 16-bit transmissions are accomplished in two 11-bit characters; the following is an example of transmissions from core locations 5325-5331:



Each bit in the special code will be echoed when received (total four characters). These echoes can be used to verify that the proper mode and address has been established. After two control transmissions, any bit pattern can be sent since they will be used only to force data out of memory (FROM mode only). The first two arbitrary 11-bit characters after the control codes (characters 5 and 6) cause the desired starting address minus one to be echoed. Since addresses are only 12 bits long, the remaining four bits (high order end of second character), where the control code is normally found, will be replaced by all one's. In the above example, the echo after the two control code transmissions will be 175324. This echo can also be used to verify that the proper starting address has been established. The next dummy character sent (character 7) will cause the least-significant eight bits of the content of core location 5325 plus the normal start/stop bits, to

be echoed; character 7 forces out of memory the first real piece of useful data. To ensure accurate transmission of data FROM the Controller, it is advisable to read data in memory twice and compare the results. Generally, this is accomplished in blocks of data, for example 64-word blocks. This allows errors to be immediately recognized and corrected before an entire memory is read with unreliable communications.

Controller Response

When data is requested in either the TO or FROM mode by the Computer Interface, the operation of the Controller is interrupted for approximately 15 microseconds to perform the requested function. This interruption is satisfied only after the Controller completes its current memory instruction; it does *not* delay until a line solution is complete or an I/O slot is serviced. Wherever it is in the scan, the Controller will stop prior to the next instruction and either load a core word or read a core word. For the worst case, an active Computer Interface will delay the scan by only 0.7% (9600 baud, continuous transmissions).

If it is desired that the Controller be shut down (stop processing data) while a large transmission takes place (such as loading a new logic program or executive) core location 7775 should be loaded with zero. Within 15 μs the Controller will be "Trapped," not scanning logic lines nor servicing I/O modules; but the Controller will be able to respond to the Computer Interface. After the reload has been accomplished and verified, the Controller can be untrapped by cycling power. To ensure proper system operation, anytime changes are made to the executive or the user logic (data line), the Controller must be trapped. If the Controller is processing data, it is possible, unless special procedures are established, to change the operation or instruction currently being executed prior to its completion, resulting in undetermined operation.

Also available from the Service Center are the exact core locations for line data, I/O Allocation Table, register values, enable tables, etc.; each of these functions vary from executive to executive and must be defined for each MOPS/TEF. In core location 3 (of all executives) is a Program Number that represents the MOPS/TEF identification (e.g., MOPS 3, Mod 13), as well as its revision level.

The keylock switch on top of the Processor will protect certain areas of memory from change even with the Computer Interface (see 3.1.4). With memory protect ON (the normal operating mode of the Controller), the Computer Interface can read the entire memory but can only change the register and I/O status area; however, trapping a Controller is possible with memory protect ON.

Options

Two options are provided with all 1646 Computer Interfaces that can be selected by connecting jumpers on the interface connector. The pin assignments for this connector are shown in Figure 125; either or both options can be selected by installing the proper jumpers. If neither option is required, the appropriate pin is simply not connected. The memory protect option is similar to the keylock switch on the Processor, except that when it is selected, it prevents the monitoring computer from writing *any* data into the Controller's core memory. The Controller basically becomes a read-only system.

The second option allows the Controller to generate a flag character to the computer. When selected, the flag option allows the next to last line in the user's program to control the generation of the flag. If the executive provides 640 lines of logic (Watchdog Timer line is line 640), line 639's coil will initiate the flag character. When the WDT-1 line is transitioned from OFF to ON, a single flag character is sent; if additional characters are required, the WDT-1 line should be turned OFF, then ON again. A timer should be used to send flags at a convenient rate (2 per second) until response is obtained from the computer. If flag characters are sent at a sufficiently high rate,

ensure that the interface has the capacity to respond to this requirement without locking out the computer. The flag character format is four zeros followed by four ones (00001111) and is transmitted in a very short time (1.1 ms at 9600 baud). If the monitoring computer is not available to respond immediately to the flag character, continuous transmissions are recommended.

If the Computer Interface is active in either a TO or FROM mode, while the WDT-1 is transitioned from OFF to ON, the flag character will be delayed until termination of the transfer. If a computer initiates a transfer while the flag character is being sent, the echo of the transfer control characters will be proceeded by the flag character.

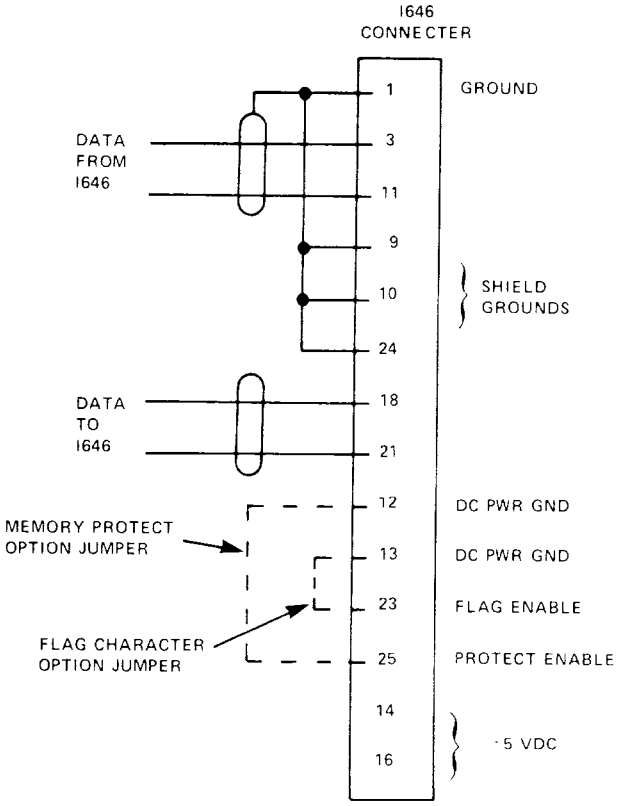


Figure 125. Pin Assignments on I646 Connector.

System Design Recommendations

In most applications, a monitoring computer system can be designed so that all transfers (except reload of executives and/or logic data) occur via the register table. This procedure allows the Controller to operate with memory protect (keylock type) ON and still provides the computer with control capability. Logic within the Controller can be designed to count parts produced, measure equipment operating times (up time), detect system

errors, etc. This data is stored in registers and thus is available to the computer for copying and can be cleared to zero if a new count level is desired. In addition, recipe data and number of batches to be produced can be loaded by the computer into registers (including input registers) for use by the Controller's logic.

If several conditions, such as error detection, end of batch, etc., can generate an interrupt (via flag character) a register should be dedicated to describing the type of interrupt. A one in this register can represent an error of type A; a two, error type B; a ten, end of batch, etc. As soon as a flag is received, the computer examines this register to determine the type of interrupt. If control of logic is required, a group of sense or calculate lines can be used to provide coil references, only when a register contains a certain bit pattern or a specific value. Of course, the contents of this register can be altered by the computer to effect control of the logic.