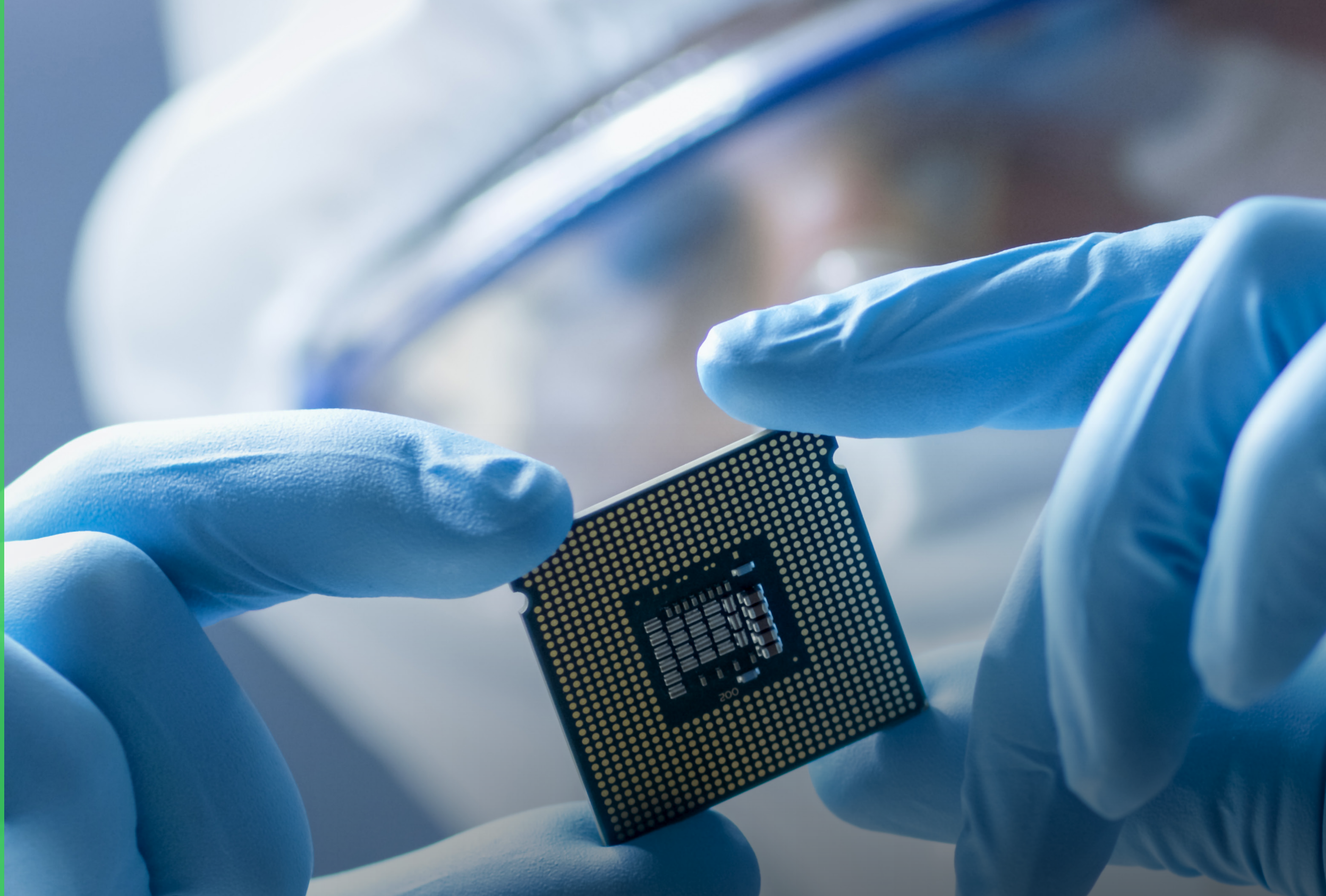
Contents



Innovative Power Solutions for Semiconductor Fabrication Efficiency

Schneider Electric Reference Guide

Life Is On | Schneider Electric

Contents

Introduction

Today, the semiconductor industry has worldwide revenues approaching $400 billion. Projections are that this number will climb substantially over the next 10 years, thanks to significant growth driven by three megatrends:

- **The Internet of Things (IoT)**
- **Self-driving cars**
- **Sustainability improvement efforts**

However, for the semiconductor industry these trends and their associated business opportunities present the challenges of reducing chip making costs while decreasing the greenhouse gas emissions produced. The semiconductor manufacturing process requires substantial consumption of electricity, so efforts to build in energy efficiency are vital. Advanced **electrical power distribution technology** in the form of automatic transfer switches (ATSs), energy efficient **uninterruptible power supplies** (UPSs), optimized electrical distribution architectures, as well as other physical infrastructure can be combined with cloud analytics to help accomplish this.

This reference guide will go over the basics of semiconductor manufacturing and the economic drivers for the industry such as the fact that the cost for a chip to perform its assigned function is always declining over time. The megatrends mentioned above will be discussed in more detail, including why they are different in nature than previous challenges the industry has faced.

The semiconductor industry has worldwide revenues approaching $400 billion.

The semiconductor industry is poised for break through global demand.

The reference guide will also describe power technology solutions, showing how these can improve business continuity. That is critical in reducing manufacturing costs because it eliminates **unplanned downtime**, which can be quite expensive. Removing this unbudgeted expense through better power management can contribute significantly to lowering manufacturing costs.

Contents

Introduction (cont'd)

Other power technology solutions can ensure the availability and quality of electricity while improving energy efficiency, thereby meeting the challenges posed by the megatrends. These technologies include solutions that protect both the upstream main incoming utility power and the downstream microprocessor dependent systems that are the basis for manufacturing.

Finally, in implementing such solutions, this guide will outline why it is important to have the right partner with the appropriate expertise. An experienced partner will make it possible to reap the benefits of energy efficient power solutions more quickly, while also ensuring business continuity. This guide will review what to look for in such a power technology partner.

Read on to discover how the semiconductor industry can take on the many opportunities and challenges of the future as well as harnessing solutions that will propel it forward.

Finding the right power technology partner is key to addressing efficiencies and ensuring uptime.

Contents

Semiconductor Industry Challenges

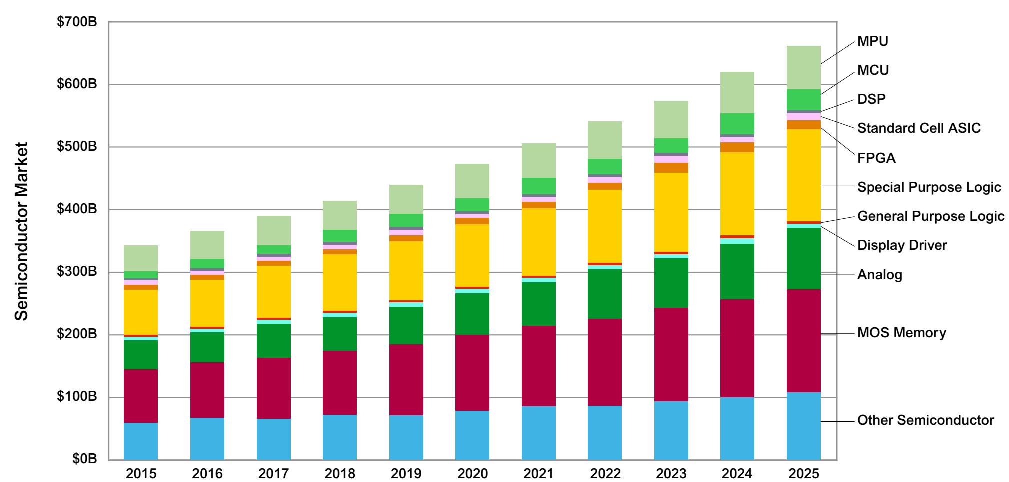
The semiconductor industry's sales were $338.9 billion in 2016, with a forecast of $346 billion in 2017 and $354 billion in 2018[1]. So, revenues are expected to grow 4.4 percent over two years. Historically, industry revenues grew at more than twice that rate from 1996 to 2016, with a **compound annual growth rate (CAGR)** of 4.8 percent[2]. The recent slowdown is due to smaller increases in the top selling segments of logic, memory and MPU semiconductors[3] arising from slower sales increases among the consumer products that require these chips. However, in looking out to 2025, predictions are for growth to again surge, with $655.6 billion in annual chip sales in 2025 and a CAGR from 2015 to 2025 of 6.7 percent[4].

In part, the surging historical sales were due to shrinking feature sizes[5], which enable chips to perform more functions at a lower cost. Another part of the cost reduction has come from increased wafer sizes, which went from 200 to 300 mm[6] from 1992 to 2002 and could in the future move to 450 mm. Bigger wafers allow more chips to be produced, resulting in manufacturing expense cuts of as much as 40 percent during the transition from one size to the next. These cost-cutting techniques are still being pursued, along with design innovations.

However, the industry today faces some unique challenges that are unlike those that have confronted it before. They come from three different fronts and are on top of the standard requirements to cut chip costs while not compromising on safety or quality. The new challenges are:

- **Internet of Things (IoT)**
- **Self-driving cars**
- **Sustainability improvement efforts**

The IoT consists of objects that are linked to other Internet-enabled devices and systems through an IP address, with the resulting connectivity allowing two-way communication between the object and devices and systems. The number of **connected devices** is growing rapidly, from 6.6 billion in 2016 to an estimated 22.5 billion in 2020. Building out the IoT will require an investment of $4.8 trillion[8], with that



Source: Handel Jones, Semiconductor Industry from 2015 to 2025, SEMI Organization, 2015

Life Is On | Schneider Electric

Contents

Semiconductor Industry Challenges (cont'd)

sum coming initially from industry and then indirectly from consumers.

Those forecasts have attracted considerable attention because they represent a significant opportunity, particularly for the semiconductor industry. Every IoT connected object, whether it is a traffic light or a cow[9,10], will need integrated circuits and there will be others in support functions. There will be sensors that capture physical measurements of interest while other chips transmit the data, although it is possible that these two functions and others will be done by a single IC (**integrated circuit**). Still other semiconductors will aggregate the data and move it to data centers, where processors will sift through everything to create actionable intelligence.

Much of the backend for the IoT is similar to what is done today for big data applications, and the increased analysis needs driven by the IoT will up the demand for semiconductors used in data centers. The sensors and other integrated circuits that go onto the objects that are the basis for the IoT are a different type of semiconductor.

The number of connected devices is growing rapidly, from 6.6 billion in 2016 to an estimated 22.5 billion in 2021.

The semiconductor industry is adapting to challenges and opportunities with shifting market demands.

For those billions of objects to be connected, the chips must be inexpensive, low-power and otherwise very light on resources. If they are not, the economics will work against the wide-spread and massive IoT deployment predicted.

Likewise, **self-driving cars** represent a significant opportunity and challenge for semiconductors. A fully autonomous vehicle will have $550 more semiconductor content than today's cars,[11] and there will be millions of them[12] produced annually within 10 years, according to analysts. However, that opportunity comes with a challenge: making the many ICs needed at a low enough cost while still ensuring that they perform in the harsh automotive environment.

As for sustainability and the need to lessen environmental impact, it is true that the semiconductor industry has long sought to minimize its resource demands for economic

Contents

Semiconductor Industry Challenges (cont'd)

Self-driving cars are accelerating demand for semiconductors with the average autonomous car requiring $550 in more semiconductor content than in today's cars.

reasons. Making a chip depends on the availability of high quality electrical power, a suitable water supply, a wafer source and appropriate raw materials.

On the other hand, the increasing attention to **climate change** and **greenhouse gas emissions** is new and represents a challenge to the industry. There is a worldwide push toward renewable energy, which the industry helps by making solar and wind power less expensive through cost cutting of components and by creating controllers that maximize energy extraction. However, there is also life-cycle greenhouse gas accounting, which evaluates and reports the full life-cycle emissions associated with the raw materials, extraction, manufacturing, transportation, use, and end-of-life management of a good[13]. This and the overall tightening down of greenhouse gas emissions called for in international agreements is new and must be accounted for in today's energy strategies.

Because semiconductors provide the brains and communication capabilities for many products, they are uniquely suited to respond to such requirements. These do place additional requirements on chips, however. The industry has started to respond to such needs, as well as looming government regulations[14].

These new demands from the IoT, autonomous vehicles and for sustainability do not change some underlying challenges. Building a semiconductor front-end 300-mm wafer fabrication facility is expensive, with the cost of a state-of-the-art plant estimated to be as high as $8.5 billion[15].

The chips to meet these challenges will be built in such fabs, as are all other semiconductors for any application. Within these costly manufacturing plants, there are numerous critical steps in the fabrication process, involving

As for sustainability and the need to lessen environmental impact, it is true that the semiconductor industry has long sought to minimize its resource demands for economic reasons.

Contents

Semiconductor Industry Challenges (cont'd)

repeated photolithography, etching, ion implantation, deposition, oxidation, and more[16]. These can be exacting, with tolerances measured in nanometers or billionths of a meter. The requirements for purity and other physical parameters of the silicon wafers are also high. Tight tolerances are also the case for device packaging and testing.

Historically, cutting chip production costs has been done by going to smaller process feature sizes, making chips on bigger wafers and integrating more functions into a semiconductor. This means that the industry faces a constant demand to innovate. For example, process feature sizes are typically given in terms of the critical dimensions of the transistor gate, and these nodes shrank by a factor of 1000 over a period of about 40 years[17]. The feature size reduction is expected to continue, thanks to improvements in **photolithography**, the incorporation of new materials and other innovations. These advances lead to a doubling of the number of transistors in dense integrated circuits every 18 months or two years, or **Moore's Law**[18].

Making a chip requires a cooperative yet competitive approach among industry players.

The market trends of IoT, self-driving cars and sustainability will press the semiconductor industry to continue to innovate and look for key operational efficiencies.

Another cost reduction option is to go to **larger wafers**, which cuts expenses by processing more chips at a time. The third way that costs can be reduced is through new designs because these may incorporate new functionality. This integration of new capabilities means that one chip may be able to do the job of several, which may make the new individual chip more expensive than the old but the overall cost of the solution lower.

In meeting these challenges, the industry is also faced with another, basic constraint. Making a chip requires a cooperative yet competitive approach among industry players. That is, the chips that will be produced a few years from now will have smaller feature sizes, incorporate new materials and possibly be built on larger wafers. They will be produced on equipment and tools that come from many different vendors. Yet, each of these systems must work

Contents

Semiconductor Industry Challenges (cont'd)

with each other as well as together. These tools are being developed today so that it will be ready some years from now when needed. In some ways, this is analogous to what must happen inside a computer. There are many different integrated circuits and they must all function as part of the whole. If they fail to do so, the computer will not work. The semiconductor industry faces the same constraint. This challenge has existed for decades and there are mechanisms to address this need. Still, it is not something that can be dismissed as trivial.

As the industry confronts new challenges in the form of IoT, self-driving cars and a focus on sustainability it must constantly innovate in a cooperative yet competitive manner. Fortunately, there are solutions to these issues, as a further examination of them reveals.

Semiconductor manufacturers continue to look for cost reductions by moving to smaller feature sizes and making other changes to decrease manufacturing costs.

Contents

Changes in the Fabrication Process

The making of a semiconductor chip involves some technological wizardry. The process starts with a common material, like sand[1], and finishes with advanced circuitry made up of many transistors, such as a microprocessor capable of executing hundreds of millions of instructions per second[2]. To accomplish this while constantly cutting the cost of a transistor or other basic electrical components, the semiconductor industry depends on an intricate and exacting process of hundreds of separate steps that involves:

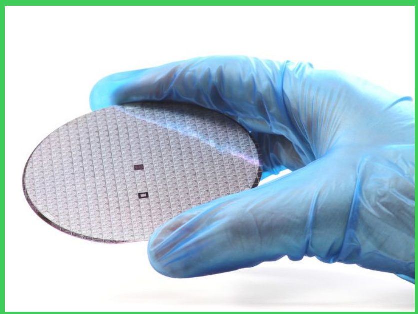
- **Silicon ingot production**
- **Front-end chip production**
- **Back-end chip production**

The continual evolution of these different aspects of manufacturing is the basis for Moore's Law, the observation that has held for decades that the number of transistors in a chip doubles every 18 to 24 months[3]. The traditional techniques behind this exploit are shrinking feature sizes, larger wafers on which the chip is built and design changes. To that, there has been the much more recent introduction of additional elements from the periodic table, innovations such as multicore processors, and what is called "**More than Moore**"[4]. The latter is a system-wide approach that incorporates new materials and devices. These traditional and "More than Moore" techniques, as well as others that may join the list, should allow chip advances to continue for the foreseeable future, although they will require changes in semiconductor fabrication. For instance, an impending change is the use of **extreme ultraviolet lithography**[5,6], a next generation technology needed to produce the finest features of chips introduced in 2019 and beyond.

Making a Semiconductor Chip

Silicon Plant

→



Wafer Fabrication
(Front-End)

→

Test and Assembly
(Back-End)

Contents

Changes in the Fabrication Process (cont'd)

Once wafers are delivered to a front-end fabrication plant, chips are then created on the wafer in a clean room where the concentration of airborne particles is controlled.

> Traditional and "More than Moore" techniques, as well as others that may join the list, should allow chip advances to continue for the foreseeable future, although they will require changes in semiconductor fabrication.

Most chips are built on silicon wafers, and for those the fabrication process starts with the pulling of a silicon ingot. This is then sliced into wafers with a diameter of as much as 300 mm[7]. According to **SEMI (Semiconductor Equipment and Materials International)** association, more than 10,700 million square inches, or 6.9 million square meters, of semiconductor grade silicon shipped in 2016[8]. That silicon was refined so that impurity levels were less than one part in 1-10 billion[9], making what started out as ordinary sand among the most highly purified products available commercially.

As part of process, the wafers are also polished so that one face is smooth and flat, with a mirror-like surface. They also have a flat notched into them, with this cutout being used in subsequent processing to orient the wafer correctly in equipment and tools. Once ready, wafers are delivered to a front-end fabrication plant. Chips are then created on the wafer in a clean room, with these areas classified according to the level of airborne particulates. Thus, a Class 100 or ISO 5 cleanroom has 29 particles of five microns size or larger per cubic meter of air while a Class 1000 or ISO 6 cleanroom has 293, 10 times as many[10].

The **front-end fabrication process** consists of many repeated steps. Typically, there is a deposition or oxidation step. Some of these operations involve metal that will be used to make circuitry wiring. Others deposit or grow silicon oxides, silicon nitrides, polycrystalline silicon or other materials. These may form insulators, conductors or a mask for the next operation.
After deposition, photolithography puts a pattern on the surface using photoresist and exposure to ultraviolet light.

Contents

Changes in the Fabrication Process (cont'd)

This is then etched or ion implanted, so that the pattern of the layer is permanently imprinted upon the chip. This can be wiring, through-holes in an insulator, transistor elements, or other chip components.

The deposition/oxidation, photolithography, etching, ion implantation and other steps are repeated over and over as the functional layers of the chip are built up one by one[11]. The entire process may end up as 250-300 separate steps, with the critical stages having tolerances measured in nanometers, or billionths of a meter, in advanced semiconductor manufacturing processes.

Semiconductor processing demands a **substantial utility infrastructure**, including ultrapure gases, dry air and nitrogen, ultrapure water, exhaust, high quality electrical power and more. Estimates are that a square meter of cleanroom may require as much as 12 square meters of infrastructure, once piping, storage and production facilities are accounted for. The ratio may be much less for some facilities.

After the chips are finished, the wafer moves to **back-end production**. This starts with a wafer sort test, which involves feeding an electrical test pattern into every chip to determine which ones are functional and which are not. The wafer is then cut into pieces, with each of these containing an individual die. The die that passed the earlier functional test moves onto the next step while those that failed are discarded.

The subsequent step is packaging, with individual die placed into a package and electrically connected to it before being sealed or protected in some way. This is the form of the chip which will be mounted on **circuit boards** and used in a product.

The semiconductor industry depends on an intricate and exacting process of hundreds of separate steps.

The economics of the situation dictate that the functional die yield should be as high as possible. Thus, there is a strong incentive to do failure analysis, figure out why a given die did not yield, and then institute changes in the process to eliminate the root cause of the problem. That is, for example, why manufacturing is done in a cleanroom, with wafers often transported between operations in an ultraclean container. Even the smallest particulate can cause a short circuit or other failure, and so achieving cleanliness on a microscopic scale is critical.

While Moore's Law has held for decades, it has taken work to keep it going and maintaining this progress has proven increasingly difficult. The problem is that the standard

Contents

Changes in the Fabrication Process (cont'd)

approach depended on shrinking chip features. Smaller features made it possible to pack more transistors on a chip, and there was the bonus that performance went up because the chips became faster and more energy efficient. Eventually, however, this ran in to the problem that insulators became too thin and spacings too close, resulting in excessive leakage. The semiconductor industry responded to this challenge by pursuing other ways in which Moore's Law could continue, along with its expectations of ever more inexpensive transistors and ever more capable chips.

> Starting around the year 2000, the number of elements of the periodic table used in semiconductor manufacturing increased substantially. Incorporating new elements changed electrical characteristics, making it possible to achieve required performance of chip speed, and power consumption.

One way was to up performance by using trace amounts of elements to tweak material properties. So, starting around the year 2000, the number of elements of the periodic table used in semiconductor manufacturing increased substantially[12]. Incorporating new elements changed electrical characteristics, making it possible to achieve required performance of chip speed, power consumption, and more. Currently, a large fraction of the periodic table is used in advanced chip manufacturing. For instance, the list has long included silicon, aluminum, oxygen, phosphorous and boron. To that, technology advances have added arsenic, gallium, indium, and the rare-earth elements cerium, europium, gadolinium, lanthanum, terbium, and yttrium[13].

Another workaround to address the difficulty of meeting Moore's Law centered on **multicore chips**, with this primarily helping processors. This addressed performance problems by splitting computational demands into separate chunks, allowing a given task to be solved in parallel by many different processor cores instead of having the same work addressed serially by a single core. The approach works but taking full advantage of it requires changes to **processor software**[14].

This expansion in elements and the use of multicore chips has been joined by what is known as "More than Moore". This takes the old idea of integration of functions that is at the heart of modern chips and extends it to areas that previously were not considered. For example, it may take micron-scale versions of discrete components such as resistors, capacitors, inductors, antennas and more, embed everything into a package, and thereby reduce total system

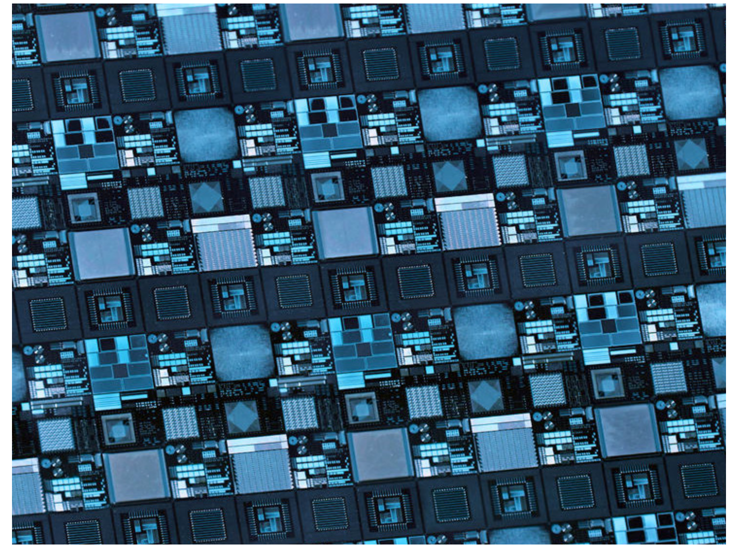
Contents

Changes in the Fabrication Process (cont'd)

size by 90 percent and cost about as substantially[15, 16]. This approach begins with the application and works its way back to the needed semiconductors and integrated circuits. In the future, there also may be a convergence of biology and chemistry with electronics when this concept is expanded to encompass even more of the entire application.

However, if this happens then it probably means changes, perhaps fundamental ones, in semiconductor manufacturing. At first, the most probable scenario is that the chip will be finished and then the other parts, such as **biological molecules**, will be added. Over time, though, such molecules may be introduced to the IC at an earlier stage of the manufacturing process.

Such a fabrication flow may seem farfetched today. On the other hand, it may not, given the technological magic already used to make today's ICs. The past evolution of chip making permits a prediction that is virtually certain to come true: significant changes in the fabrication process loom.



Close-up view of a silicon wafer.

Contents

Megatrends Impacting Semiconductor Growth

In 2017, worldwide semiconductor revenues topped $346 billion, an increase from the previous year of 2.1 percent.[1] Market analysts noted that this healthy growth came despite a small increase in traditional markets, such as smartphones and PCs. Looking forward, non-traditional applications in the industrial, automotive, and storage markets will drive semiconductor sales.[2]

Three emerging megatrends are impacting future semiconductor industry growth trajectories:

1. The **Internet of Things (IoT)**, a rapidly growing network of physical devices, vehicles, home appliances and other items embedded with electronics, software, sensors, actuators, and networks which enables these objects to connect and exchange data.
2. The forecasted growth in new **self-driving vehicles**.
3. The growing emphasis on increased **sustainability efforts in manufacturing**, through an agreement to uphold higher emissions standards, reached in Paris in 2015 at COP21.[3] Each of these megatrends will impact semiconductor fabrication, design and usage as well as the market for chips.

IoT is driving growth in the use of sensors, communication devices and other chips that are either built-in or added to objects. The number of IoT devices is projected to reach 22.5 billion in 2021, up from 6.6 billion in 2016.[4] In terms of sales, the forecast is for semiconductor revenue to grow from $94 billion in 2016 to $172.8 billion in 2025. That represents a compound annual growth rate (CAGR) of seven percent.[5]

The number of IoT devices is projected to reach 22.5 billion in 2021, up from 6.6 billion in 2016.

In contrast, the growth in PCs has been flat or negative for years,[6] a trend that shows no sign of changing. Smartphone sales are sluggish, with a five-year compound annual growth rate of only 3.3 percent.[7] Thus, the drivers of past semiconductor revenue increases continue to be important, but they are not a source of future growth.
The second megatrend, autonomous vehicles, represents a

The Internet of Things (IoT) is dramatically driving increased semiconductor revenue growth.

Megatrends Impacting Semiconductor Growth (cont'd)

market which is expected to grow from $3.6 billion in 2015 to $65.3 billion in 2027.[8] Radar and associated electronics are expected to be the fastest growing part of the self-driving car market. The radar sensors must be compact, perform well and be relatively inexpensive, at least as compared to radar sensors used in aerospace. Other semiconductor heavy applications include cameras and communications. GPS modules used to locate vehicles will also contain significant semiconductor content.

Today's cars have about $330 in semiconductors per vehicle. Estimates are that partial automation will add about $100 to that figure while full automation will increase the semiconductor value by about $550.[9] An automotive device must operate, for instance, in temperatures ranging from -40° to +125°C.[10] That is a far wider operating temperature range than that of consumer devices. Again, this

Sustainability efforts will continue to drive process improvement and increase demand for sensors and processors to reduce overall energy usage.

Today's cars have about $330 in semiconductors per vehicle.

megatrend places a premium on improved semiconductor fabrication operational efficiency, realized through mitigating unplanned downtime.

The sustainability megatrend impacts semiconductors in two ways. Semiconductors reduce demand for power and fuel and improved control of building heating, cooling, ventilation and lighting. In addition, traffic control of cars on the ground will need to reach the same level of precision as what we see for planes in the air. The sustainability trend also drives a growth in initiatives for reducing the energy needed to design, manufacture, utilize, and then dispose of a semiconductor.

Increased uptime across semiconductor manufacturing lines through modernization, digitalization and more advanced power protection lowers overall cost because up to half of the expense of making a chip is due to depreciation of the equipment and the building.[11] Improving business continuity through the reduction of unplanned downtime helps meet the challenge posed by these three megatrends.

The three megatrends facing the semiconductor industry are only partly responsible for the fundamental

Contents

Megatrends Impacting Semiconductor Growth (cont'd)

While the costs of purchasing and operating their equipment is high, another significant source of expense for semiconductor manufacturers is unanticipated downtime.

economic changes that are taking place. Over the last 50 years, the industry has benefited from Moore's Law (an observation made during the mid-1960's that the number of transistors in a dense integrated circuit will double approximately every two years in the foreseeable future). An effect of **Moore's Law** is that the cost of computation, sensing or other measure of useful work always declines. Consequently, the capability of chips always increases, which in turn leads to an ever-widening circle of applications.

This virtuous cycle, however, may be coming to an end. Today's advanced chips have features 300 times smaller than those that represented the state-of-the-art 40 years ago.[12] This ongoing reduction in size is increasingly difficult to attain, and this is one of the main reasons why the cost of processing equipment and wafer fabs has risen. As innovations such as biological or chemical molecules within chips disrupt the traditional process, the adjustments needed to continue fulfilling Moore's Law in the future may prove to be technically possible but not cost effective.

One way in which semiconductor fabrication operational efficiency (and accompanying energy cost reductions) can be improved is through the minimization or elimination of unplanned downtime.

Semiconductor manufacturing companies spend billions of dollars each year to keep their existing facilities up-to-date. Roughly 75 percent of their total expense is in equipment. The machines and physical infrastructure that support the cleanrooms required for the delicate manufacturing of semiconductor chips, along with supporting power, water, and ventilation infrastructure represent a significant capital expense (CapEx). The equipment also generates significant operating expense (OpEx) costs related to power consumption and maintenance.

The cost of a single next-generation EUV (extreme ultraviolet) photolithographic stepper, for example, runs between $90-120 million,[13,14] and many such steppers are needed. Ion implanters also cost millions of dollars each, and every silicon wafer requires as many as 30 implants.[15] A large wafer fab facility may process up to 50,000 wafers a month, and so it must have dozens of implanters busily working within it to achieve that output. Power outages, surges and sags can damage such highly sensitive equipment, driving up maintenance costs and increasing the risk of fouling wafers under production.

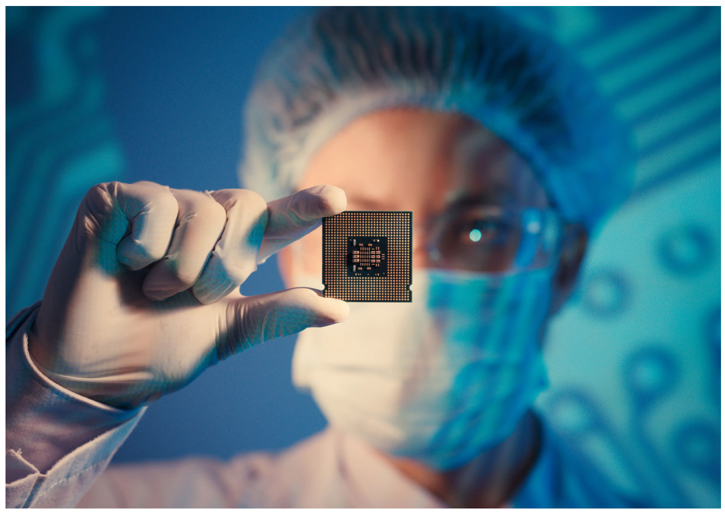
While the costs of purchasing and operating their equipment is high, another significant source of expense for semiconductor manufacturers is unanticipated downtime. Some chip manufacturing steps involve high temperature processing and such delicate operations cannot be safely

Contents

Megatrends Impacting Semiconductor Growth (cont'd)

interrupted. Having to scrap production will result in significant loss.

Within a multibillion dollar wafer fabrication plant, unplanned downtime can run into the millions of dollars per hour in losses. Thus, semiconductor manufacturing processes need to be analyzed to minimize downtime risk exposure.



Unplanned downtime can result in millions of dollars an hour in losses from such factors as lost production and lost inventory.

Many opportunities exist to reduce downtime risk, but perhaps the most significant are those that also lower the risk of premature equipment wear due to temporary power sags, swells or interruptions. These solutions minimize the effect of power problems through power conditioning and power back up solutions and also offer sensible options for coping with the longer duration problem of a power outage.

Implementation of these solutions raise semiconductor fabrication operational efficiency by eliminating work stoppages due to such issues as voltage irregularities or other power glitches and protect expensive equipment.

Within the semiconductor industry, the issue of power quality has grown in importance as equipment becomes more automated and under the control of microprocessors. Trade associations such as **SEMI** (Semiconductor Equipment and Material International), help to develop specifications and standards (like the community developed **SEMI F47 Voltage Sag Immunity standard**[16]) that address equipment-related concerns such as how to deal with unstable power sources.

Contents

Semiconductor Business Continuity Solutions

Semiconductor manufacturing is capital intensive, with a state-of-the-art wafer fabrication site costing billions of dollars and companies investing more than $10 billion yearly to keep manufacturing technology and facilities up-to-date.[1] One result of this heavy investment in plants and equipment is that depreciation is quite significant, perhaps as much as half the cost it takes to manufacture an IC.[2]

Depreciation adds to the cost of a chip, even when a manufacturing process is idle. Consequently, maximizing semiconductor manufacturing uptime is critical. Maintaining uptime spreads the depreciation burden over more ICs, and therefore reduces the cost of those chips. Megatrends like the Internet of Things (IoT), self-driving cars and the requirement to improve sustainability will increase the demand for low-cost chips, and will require higher chip performance at no additional cost. This will force the semiconductor industry to become more energy efficient.

Efforts to eliminate unplanned downtime will maximize production and cut costs. Semiconductor manufacturing relies on a variety of resource inputs, with one of the

> In most cases, for mission critical applications, a backup power scheme is in place should an unanticipated disruption to utility or mains power occur.

Addressing ways to improve business continuity is critical and will lead to increased productivity and decreased costs.

most critical being electrical power. The **chip fabrication process**, for example, consists of as many as 300 steps executed by such tools as ion implanters, photolithographic steppers, deposition systems, oxidation furnaces, etchers and more.[3] This equipment requires a clean, stable supply of electricity to run. The increasing use of microprocessor controlled, sensor equipped, and communication capable equipment means that tools are more and more sensitive to the quality of the electricity. Voltage fluctuations, such as a sag when heavy loads switch on or off, can trigger problems for tools like ion implanters or photolithographic steppers. These tools process the wafers one at a time, sequencing them through steps that begin with selecting a wafer from a stack of incoming wafers, aligning the selected wafer, performing an operation on it, and then moving it forward to join others that have completed the processing step. All of this is performed under the direction of a processor acting as a controller, which depends upon sensors, actuators, pumps, material handling equipment

Contents

Semiconductor Business Continuity Solutions (cont'd)

Unplanned Downtime Risk Assessment: Determine the Need for a UPS

What equipment, processes or operators need protecting?

- What are the safety implications of an unplanned shutdown?
- How expensive is unplanned downtime?
- What production or equipment is impacted?
- What happens if a generator fails to start?

What power quality events need to be covered?

- How sensitive is the equipment or process?
- Event types: voltage interruption, voltage spikes/dips, voltage sags
- Event length: milliseconds, minutes, hours

What does it take to recover from a downtime event?

- How straightforward is it to restart the process (time and intervention)?
- What is the effect on upstream and downstream systems?
- Is the system data potentially lost during the downtime event recoverable?

and more. Voltage problems can impact any part of this control-and-action chain. Power quality can also impact other parts of manufacturing, such as plant Ethernet and facilities control, and emergency and security systems. If equipment in any of these areas fails due to power quality, then the manufacturing process may be impacted, and process efficiency decreased. The effect will be an increase in manufacturing cost, with this happening in an environment where the need for high process efficiency has never been greater.

What are some of the business continuity- related power solutions that address these issues? As power comes into the facility from the utility, the power distribution system converts the utility power, or mains (through step down transformers, for example) so that both **medium voltage** (MV) and **low voltage** (LV) equipment can have the power it needs to safely operate. In some cases, the facility might have access to multiple sources of utility power, although this is rare. In most cases, for mission critical applications, a backup power scheme is in place should an unanticipated disruption to utility or mains power occur.

Devices such as **automatic transfer switches** (ATS), **uninterruptible power supplies** (UPS) and diesel or natural gas generators all play an important role in these backup schemes. An ATS can reroute the flow of power based on preconfigured rules so that power can continue to flow despite changes in the power infrastructure. A UPS senses when the mains power gets cuts and the internal circuitry is fast enough to temporarily assume the power load in a way that downstream devices are not affected. The UPS then uses the power stored in its batteries to act as a temporary bridge until power to the mains is restored or until gas and/or diesel generators can be fired up to support the load (until the mains power is restored). The intelligence built into these systems is what enables the transfer of power across these various mediums at the right time.

UPSs are also helpful in managing less severe power anomalies (above and beyond their duty of managing

Semiconductor Business Continuity Solutions (cont'd)

An uninterruptible power supply (UPS) is a critical component of system power backup plans. (Schneider Electric Galaxy VX)

power outages). These other functions include mitigation of harmonics (electrical distortion powerful enough to disrupt the functioning of sensitive equipment), and stabilization of power supply to the load when power dips and voltage or frequency sags occur.

These power protection techniques are widespread in the semiconductor space, with integrated solutions that provide power monitoring and resilient architectures that improve sub-function operations. A well-designed power architecture can optimize the use of energy and save up to 30 percent in operating energy costs[4].

In addition to the "upstream" protection of the facility power or "mains" coming in from the utility, there is also a need to protect equipment further "downstream" that hosts the higher intelligence that permits the sophisticated equipment within the semiconductor plant to operate. Such "brains" applications that would typically require power protection include:

- **Machine and process controls:** PLC (programmable logic controller), DCS (distributed control system), HMI (human machine interface), instrumentation and safety controls

- **Remote manufacturing IT:** SCADA (supervisory control and data acquisition), MES (manufacturing execution system) servers, plant industrial PCs, control rooms

- **Plant Ethernet:** protecting this is more important than ever, given the increasing connectivity of systems in the wafer fab and elsewhere in the semiconductor manufacturing process

- **Facilities control:** building management systems, power monitoring and control

- **Emergency systems:** lighting and fire suppression

- **Security systems:** access control, cameras, and DVRs. When deploying power protection solutions, the process begins with an analysis of the needs of a specific application (whether that be large or small). For example, a host terminal may only require the support of a shoe-box sized single-phase 1 kVA UPS. Conversely, a furnace may need a refrigerator-sized three-phase UPS with as much as 500 times the capacity[5] to ensure that wafers are not subjected to the thermal shock of a sudden cool down.

In general, larger UPSs are more commonly used for front-end chip fabrication than they are for back-end chip production. The former is where the most power-hungry process tools are located, along with exhaust, water,

Contents

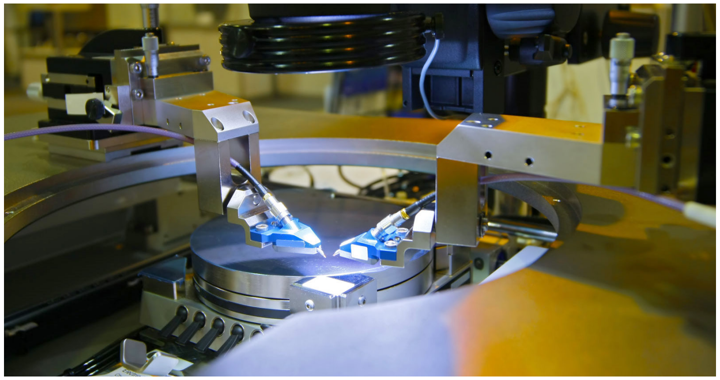
Semiconductor Business Continuity Solutions (cont'd)

compressed air, nitrogen, and process gas utilities. Front-end chip production is characterized by hundreds of steps, with these involving many tools and utilities. Ideally, all areas and tools in the front-end will be protected.

Back-end manufacturing, in contrast, consists of wafer sort test and slicing, followed by packaging and final testing[6]. In this part of the plant, there are fewer steps and tools and not as much power is required to continue to operate or to come to a safe status should an extensive power failure occur. Thus, the required UPS will, in general, be smaller.

Regardless of the situation, a business continuity solution should comply with SEMI F47, a standard for voltage sag immunity.

However, there is an important point to consider when evaluating business continuity solutions for the back-end area. The chips at this point are of higher value than they are earlier in the process. Therefore, the economic payoff of protection of this inventory is higher. Also, it may be possible to satisfy the needs of the entire, back-end production site with a single UPS. In that case, the UPS may be large, perhaps larger than anything deployed on the front-end.



Uninterruptible Power Supplies (UPS) need to be configured according to the needs of a specific application.

Regardless of the situation, a business continuity solution should comply with SEMI F47, a standard for voltage sag immunity[7]. Developed jointly by interested members of SEMI (Semiconductor Equipment and Materials International), F47 is applicable to the manufacturing process (but not to utilities equipment). It specifies that for durations ranging from 0.05 to 1.00 seconds, equipment should be immune to voltage drops of 50 percent of nominal for the shortest duration and as much as 20 percent voltage sag for the longest duration. To satisfy these requirements, equipment manufacturers often incorporate a UPS (although the specification does not require a UPS).

It is also important to realize that SEMI F47 by itself does not ensure continuous equipment service. This is another reason why UPS technologies are a prudent addition to any business continuity plan in order to assure that operational uptime is secured should a power disruption occur.

Contents

Critical Power Solutions Address Megatrends

As the major market trends of the Internet of Things (IoT)[1,2], self-driving cars[3,4], and greenhouse gas emission reductions[5] grow in influence, many semiconductor manufacturers will need to rethink how their factory infrastructures are equipped to handle the "new normal". Due to shifting demand and additional business opportunities, semiconductor facilities will need to align their operations to accommodate both increased speed-to-market requirements and to efficiently phase in the growing wave of emerging technologies. Although these megatrends present the semiconductor industry with new and expanded market opportunities, new challenges in cost reduction will need to be addressed.

One important area where factory production downtime costs can be better controlled is through the deployment of appropriate critical power solutions. A large wafer fab, for instance, can consume as much as 100 megawatts of power, making it more energy intensive than many automotive plants and oil refineries[6]. A wafer fab can use as much water as a small city[7], and is also resource intensive in the areas of gases, chemicals, and wafers. In fact, energy and resource consumption has become such a concern that the industry has now developed standards to measure energy usage and evaluate a **fabrication plant's carbon footprint**[8].

Electricity can account for up to 30 percent of a wafer fab's operating costs in some markets

Newer Internet of Things applications from self-driving cars to agriculture industry applications like soil and livestock monitoring are driving up demand for semiconductor production.

However, as semiconductor manufacturers are confronted with the need to produce chips with ever smaller feature sizes, operations-driven resource usage is likely to increase dramatically. For instance, the next generation of steppers under development for use in the most advanced wafer fab manufacturing processes employ EUV, or extreme ultraviolet, lithography. These technologies may require 10 times the power of the previous generation[9], in part because of a low conversion efficiency (of only a few percent) of an infrared pump laser into the desired ultraviolet output[10].

Better water management is another way to shrink carbon footprint chip fabrication. Water, when used in

Critical Power Solutions Address Megatrends (cont'd)

The semiconductor industry needs to improve energy efficiency and water management in manufacturing to reduce its carbon footprint.

semiconductor manufacturing, is classified as ultra-pure[11]. It is devoid of organic and inorganic contaminants. This purification process requires energy intensive filtering and treatment. The electricity consumed by pumps, motors, drives and other infrastructure that moves the ultrapure and waste water in, around and out of the wafer fabrication facility is also significant.

Any such carbon emissions reduction activities can work together with cost-cutting initiatives. Electricity can account for up to 30 percent of a wafer fab's operating costs in some markets[12]. Savings through improved energy efficiency, therefore, can help cut the cost of making a chip while improving sustainability.

How are these energy savings and accompanying benefits to be realized? The answer lies in careful evaluation of the manufacturing process and operation, looking for areas where savings can accrue. Follow that by implementing solutions, measuring results and repeating the process as needed.

When it comes to evaluation, studies have shown that wafer fabrication plants may be overengineered. For example, the movement of a large volume of air through the cleanroom requires the maintenance of a certain level of air pressure. However, in many cases, this ventilation may be excessive, and energy is being wasted without any improvement in chip yield, fab performance, worker safety or other figure of merit.

In the realm of power protection and energy management for business continuity, the impact of deployment of Uninterruptible Power Supplies (UPS) either upstream at the facility level, or further downstream at the manufacturing line level, should be measured in both minutes of downtime per year and in annual energy cost savings.

Contents

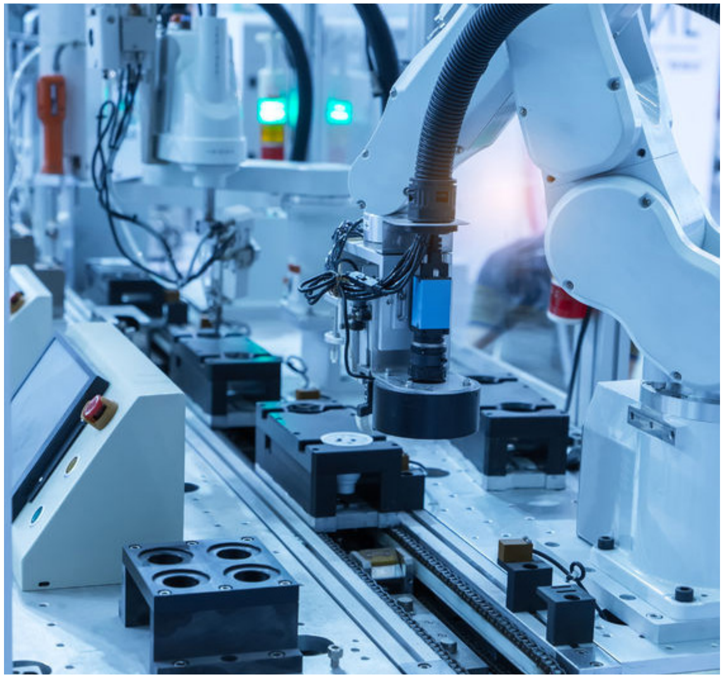
Critical Power Solutions Address Megatrends (cont'd)

To take another example, in the realm of power protection and energy management for business continuity, the impact of deployment of Uninterruptible Power Supplies (UPS) either upstream at the facility level, or further downstream at the manufacturing line level, should be measured in both minutes of downtime per year and in annual energy cost savings. Older UPSs may only be 89 percent efficient while some of the new models can operate at more than 99 percent efficiency. Such a difference can result in hundreds of thousands of dollars in savings each year.

Factory wide, by following such techniques, energy costs can be reduced substantially. In fact, electricity consumption can be cut by up to 30 percent[14] by deploying more efficient power protection technologies, as well as through power monitoring, deployment of resilient power architectures, and optimization.

In fact, in this age of **digitized components**, the need for designing and implementing a comprehensive power architecture helps maximize the benefits of advanced connectivity. An important key for managing IoT-driven semiconductor factory control automation, of which power is an important component, is to view the cloud, edge, and on-premise plants as part of a larger whole that is built upon an open, multi-layered architecture. When piecing together such an architecture, a holistic view should be taken and development planned in the aggregate, with the application and the physical environment being central considerations.

Fortunately, there's no need for control engineers to reinvent the wheel by architecting a digital infrastructure from the ground up. Physical infrastructure companies like Schneider Electric have developed vendor-neutral, validated architectures (which Schneider Electric calls "**EcoStruxure™**") that include an open but tailored stack of connected products, control level software, and cloud-based services for supporting applications and data analytics. Such platforms are made accessible to developers and to a wide ecosystem of partners so that systems are more agile, flexible and secure. This common platform/open architecture/open ecosystem approach accommodates information technology (IT) and operations



A comprehensive power architecture helps maximize the benefits of advanced connectivity which is important in managing IoT-driven semiconductor factory control automation.

Life Is On | Schneider Electric

Contents

Critical Power Solutions Address Megatrends (cont'd)

New open architectures of connected products, edge control, apps, analytics and services now interoperate across the domains of industrial companies and help drive measurable profitability in the three domains of safety, efficiency and reliability.

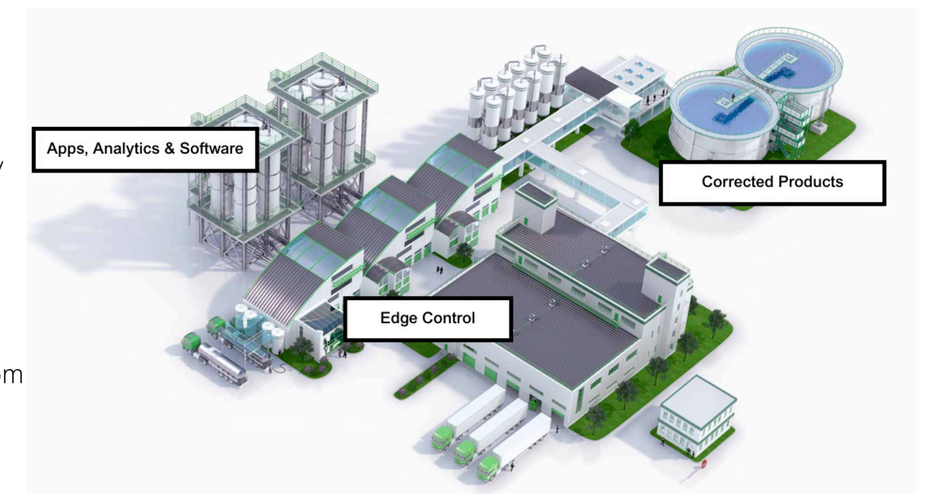
technology (OT) equipment and software and IoT-oriented solution development.

Such a comprehensive architecture of innovative digital technologies allows companies to seamlessly connect, collect, analyze and act on data in real time to improve safety. This type of platform allows for much easier management of core manufacturing processes across the key elements of **cloud, edge, and on-premise**. Operators, for instance, can view cloud connected critical data anytime, anywhere from any device. Resiliency and visibility are improved through live sensor data, predictive analytics, and smart alarming. Operators also have access to experts monitoring connected assets 24/7.

Deployable both on-premise and in the cloud with built-in **cybersecurity** at each architectural level, users can perform real-time corrective actions in the short term and optimize their whole ecosystem in the long term. This results in better decisions which directly increase the profitability of the business.

This improves the agility of organizations by enabling key process owners to respond more quickly to market dynamics. By providing a collaborative workspace that connects applications and analytics to the field systems/devices, the architecture allows teams to view combined intelligent dashboards in real-time, enabling faster and more accurate decisions.

These new **open architectures of connected products**,



An open architecture or open ecosystem approach accommodates information technology (IT), operations technology (OT) equipment, software and IoT-oriented solution development.

Life Is On | Schneider Electric

Contents

Critical Power Solutions Address Megatrends (cont'd)

edge control, apps, analytics and services now interoperate across the domains of industrial companies and help drive measurable profitability in the three domains of safety, efficiency and reliability.

Such an architecture brings **IT** and **OT** together making it possible to analyze a wafer fab's operation because it feeds the raw data from the plant floor into the analysis tools of the office. This makes it possible to comb through the hundreds of steps involved in wafer fabrication with an eye toward identifying trends that consume and possibly waste the most energy. Linking IT and OT then makes it feasible to adjust processes and steps that waste energy while providing the means to make sure any changes being made do not adversely impact the finished product or fab operations.

The process of evaluation of operations, devising an improvement plan, implementing it, and then measuring the results can be repeated as needed until the desired energy savings are achieved. Chip fabrication is a complicated process, with many exacting steps where critical tolerances are measured in nanometers. For that reason, it takes technical expertise to determine if a given change in energy usage is likely to have a negative impact.

It is equally important that power solutions not lead to other issues. In a highly connected environment, for example, a failure in any system can cause a process step, the entire manufacturing process, or a plant to go out of sync. So, an improperly managed back-up power system or other infrastructure components can also create problems. Therefore, a proactive monitoring and maintenance strategy for power and control systems should be

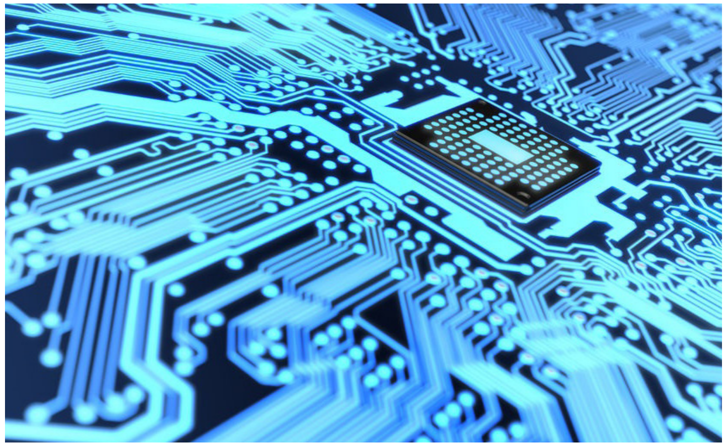
Bridging Information Technology and Operations Technology is vital to improve processes while ensuring any changes do not adversely impact the finished product or fab operations.

established because that will ensure the ongoing continuity of operations.

The cost- and emission-reduction challenges facing the semiconductor industry arising from the IoT, self-driving cars, and sustainability can be addressed through the implementation of critical power solutions. An architecture that includes upstream and downstream power protection, improves manufacturing line availability and the overall quality of power.

Contents

New Industry Demands Require New Solutions



Ensuring uptime is mission critical in the semiconductor industry.

The semiconductor industry is facing new demands due to three megatrends: the IoT, self-driving cars, and a requirement to improve sustainability. Power solutions can help meet these needs by decreasing unplanned downtime, reducing the chance for scrap and improving **energy efficiency**. These outcomes are easier to achieve when critical and business continuity power solutions are deployed in conjunction with a knowledgeable partner that possesses the required expertise.

The changes confronting the semiconductor industry arise from an evolving market. In the past, growth was primarily in consumer or enterprise products, with examples being PCs, smartphones, televisions and servers. However, over the next decade the fastest growing market segments will be in the industrial and automotive sectors[1,2,3]. Fueling this new growth is the Internet of Things (the IoT) which is driving the need for low-cost sensor and communication chips as billions of devices connect objects to the Internet[4].

Self-driving cars will also need large quantities of chips. By some estimates a fully autonomous vehicle increases the semiconductor content by 267 percent as compared to today's cars[5].

The final contributor to the evolving market is the need to increase sustainability in semiconductor manufacturing and for industrial applications, transportation, buildings and more. This flows from the international agreement reached to limit greenhouse gas emissions such that any future temperature change is much less than 2º C above pre-industrial levels[6]. As a result, energy efficiency will need to improve, which means that ICs will be in demand for sensing, control and communication. Importantly, this will happen while the entire semiconductor manufacturing chain – silicon ingot, front-end and back-end production – is also called on to improve energy efficiency. A front-end production facility, a wafer fabrication plant, uses about as much power as 50,000 homes and some of the largest consume more electricity than an auto manufacturing

A front-end production facility, a wafer fabrication plant, uses about as much power as 50,000 homes and some of the largest consume more electricity than an auto manufacturing plant.

Contents

New Industry Demands Require New Solutions (cont'd)

plant[7]. That fact will make such facilities and others involved in semiconductor manufacturing subject to regulations aimed at limiting climate change.

These challenges are in addition to others faced by the industry, such as the need to innovate by going to smaller feature sizes, moving to bigger wafers, incorporating new materials and developing new designs. Those advancements lead to changes in the semiconductor fabrication process, with an example being the current rollout of EUV (extreme ultraviolet) lithography after decades of research and development[8]. The cost of advanced processing equipment can run over $100 million each[9], and many such tools will be needed in every wafer fabrication factory. That is one of the reasons why most of the investment in a wafer fabrication plant is in the power-intensive equipment.

The need to innovate means that no one company can supply all the tools and techniques needed to produce a chip or advance the state-of-the-art. Instead, this must be done by the entire semiconductor manufacturing ecosystem. Thus, smaller players can influence the industry direction by working through industry trade associations, like SEMI (Semiconductor Equipment and Materials International), and the technical committees/ task forces formed by a trade association to address the problems confronting the industry. This opportunity may be even greater in the future, as the industry's makeup changes due to the rise of fabrication sites and major players in South Korea, Taiwan, China, and elsewhere[10,11].

These challenges and opportunities in the market can be also addressed by partnering with a knowledgeable power partner who can provide holistic and innovative solutions. One example of a total solution approach can be found with Schneider Electric's EcoStruxure™ solution. This comprehensive solution improves availability, security, efficiency and asset management for semiconductor manufacturers.

Critical power and business continuity solutions can help address the three megatrends as well as the ongoing need to innovate while continuing to manufacture quality products safely. The cost structure of semiconductor manufacturing means that downtime is expensive. Because depreciation alone can contribute as much as half the cost of making a chip[12], keeping equipment up and running is of paramount importance. The connected nature of modern factories means that this need for enhanced uptime extends beyond what has traditionally been protected through automatic transfer switches (ATS),

The cost structure of semiconductor manufacturing means that downtime is expensive. Because depreciation alone can contribute as much as half the cost of making a chip, keeping equipment up and running is of paramount importance.

Contents

New Industry Demands Require New Solutions (cont'd)

uninterruptible power supplies (UPS), backup generators and other technology aimed at incoming utility or mains power. Instead, what is needed now for business continuity is additional protection of any microprocessor controlled equipment through the use of a UPS, an uninterruptible power supply. This will ensure the equipment meets the **SEMI F47 voltage sag immunity specification** while also improving business continuity and reducing the chance of wafers being scrapped due to a power failure.

This is all part of a total solution approach. EcoStruxure™ is Schneider Electric's IoT-enabled, open, interoperable architecture and platform. It offers a tailored stack of connected products, control level software, and cloud-based services for supporting applications and data analytics. Such a holistic solution improves business continuity and efficiency.

Critical power solutions can also help improve efficiency within the manufacturing process, a need that SEMI recognizes and has addressed through energy measurement standards S23 and E6[13]. The potential operational energy savings are as much as 30 percent[14], which together with greater business continuity and process efficiency can translate into a significant cost reduction.

Innovations will be driven by many companies and organizations in the entire semiconductor manufacturing ecosystem, as one company can't supply all the tools and techniques needed to produce a chip or advance state-of-the-art manufacturing.

Contents

Resources

Business Solutions

Schneider Electric EcoStruxure™ Platform for IoT used in Semiconductor Segment Applications

Industrial Business Continuity Solutions

Semiconductor Secure Power Solutions

Ensuring Process Continuity in Your Semiconductor Fabrication

Blogs

Critical Application Protection Vital to Ensure Continued Operations in Semiconductor Production

Making Semiconductor Production More Energy Efficient

How Cooperation and Trade Associations Push the Semiconductor Industry Forward

Semiconductor Megatrends are Driving the Need for Critical Power Solutions

How Power Solutions Help Semiconductor Manufacturers Address Cost, Safety and Quality

Why Fit-for-Purpose Power Solutions are Required for Semiconductor Manufacturing

3 Key Steps to Maximizing Uptime for Mission Critical Systems

Contents

Footnotes

Chapter 2: Semiconductor Industry Challenges

1. SIA Factbook 2017
2. Ibid
3. Ibid
4. Handel Jones, International Business Strategies, SEMI Whitepaper "Semiconductor Industry from 2015 to 2025"
5. Wikipedia "14 nanometer" entry
6. F450 infographic
7. Business Insider Intelligence, "The Internet of Things 2017 Report"
8. Ibid
9. WhaTech, "IoT market in livestock management to report 12.14% CAGR by 2021"
10. TechRepublic, "IoT for cows: 4 ways farmers are collecting data from cattle"
11. Pete Singer, Semiconductor Manufacturing & Design, "Infineon CEO Says Robot Cars Will Drive Semiconductor Demand"
12. "Autonomous Vehicles Market Size to Observe Steady Growth and Industry Expected to Grow USD 3.6 billion with CAGR 26.2% by 2027"
13. EPA, "Life-Cycle GHG Accounting Versus GHG Emission Inventories"
14. SEMI, "Semiconductors and Sustainability"
15. Max Chafkin and Ian King, Bloomberg Businessweek, "How Intel Makes a Chip"
16. Intel, From Sand to Silicon
17. Wikipedia "14 nanometer" entry
18. Moore's Law

Chapter 3: Changes in the Fabrication Process

1. Intel, From Silicon to Sand
2. Wikipedia, Instructions per second
3. Moore's Law
4. M. Mitchell Waldrop, "The chips are down for Moore's law," Nature
5. ASML, **EUV production insertion: Factors to Watch**
6. Wikipedia, Extreme ultraviolet lithography
7. F450C, "Evolution of the Silicon Wafer Infographic"
8. SEMI, "Silicon Shipment Statistics"
9. Norman Greenwood and Alan Earnshaw, **"Chemistry of the Elements"**
10. Terra Universal, FS209E and ISO Cleanroom Standards
11. Intel, From Sand to Silicon
12. Electronics Weekly.com, "Periodic table is key to semiconductor advances"
13. Wilburn, D.R., 2012, "Byproduct metals and rare-earth elements used in the production of light-emitting diodes—Overview of principal sources of supply and material requirements for selected markets: U.S.
14. Larry Hardesty, "Smarter multicore chips"
15. M. Mitchell Waldrop, "The chips are down for Moore's law," Nature
16. Rao R. Tummala, "Moore's Law Meets Its Match," IEEE Spectrum

Chapter 4: Megatrends Impacting Semiconductor Growth

1. **SIA Factbook 2017**
2. Gartner, **"Gartner Says Worldwide Semiconductor Revenue Forecast to Grow 7.2 Percent in 2017"**
3. **Sustainable Innovation Forum 2015**
4. Business Insider Intelligence, **"The Internet of Things 2017 Report"**
5. IHS Markit, **"Semiconductors in the IoT"**
6. Charles Arthur, The Guardian, **"PC market doldrums will continue to 2018, says IDC"**
7. IDC, **"Smartphone Growth Expected to Remain Positive as Shipments Forecast to Grow to 1.7 Billion in 2021, According to IDC"**
8. **"Autonomous Vehicles Market Size to Observe Steady Growth and Industry Expected to Grow USD 3.6 billion with CAGR 26.2% by 2027"**
9. Pete Singer, Semiconductor Manufacturing & Design, **"Infineon CEO Says Robot Cars Will Drive Semiconductor Demand"**
10. Intel, "The Automotive-Grade Device Handbook"
11. Russ Fischer, **"Intel and Micron and Depreciated Fabs"**
12. Wikipedia **"14 nanometer"**
13. Peter Clarke, Electronics 360, **"TSMC Orders EUV Lithography Tools for Production"**
14. Mark LaPedus, EE Times, **"EUV tool costs hit $120 million"**
15. Leonard Rubin and John Poate, The Industrial Physicist, **"Ion Implantation in Silicon Technology"**,
16. **SEMI F47**

Chapter 5: Semiconductor Business Continuity Solutions

1. The Inquirer, "TSMC says 3nm plant could cost it more than $20bn"
2. Russ Fischer, **"Intel and Micron and Depreciated Fabs"**
3. Intel, From Silicon to Sand
4. Schneider Electric, **Semiconductor Secure Power Solutions**
5. Ibid
6. Intel, From Sand to Silicon
7. SEMI F47- Voltage Sag Immunity Standard Reapproved

Footnotes (cont'd)

Chapter 6: Critical Power Solutions Address Megatrends

1. Business Insider Intelligence, **"The Internet of Things 2017 Report"**
2. IHS Markit, **"Semiconductors in the IoT"**
3. **"Autonomous Vehicles Market Size to Observe Steady Growth and Industry Expected to Grow USD 3.6 billion with CAGR 26.2 percent by 2027"**
4. Pete Singer, Semiconductor Manufacturing & Design, **"Infineon CEO Says Robot Cars Will Drive Semiconductor Demand"**
5. **"Historic Paris Agreement on Climate Change"**
6. Steve Chen et al, McKinsey, **"Bringing energy efficiency to the fab"**
7. IEEE Spectrum, **"Semiconductor Manufacturing Plants can use as much water as a small city."**
8. **Reducing Energy and Carbon Footprint at Fabs: A New Focus for SEMI Standards**
9. Wikipedia, **Extreme ultraviolet lithography**
10. Andreas Thoss, **"The secret of EUV generation"**
11. Pure Water Group, **Electronics grade water**
12. Steve Chen et al, McKinsey & Company, **"Bringing energy efficiency to the fab"**
13. Schneider Electric, **Semiconductor Secure Power Solutions**
14. Ibid
15. Schneider Electric, **Ensuring Process Continuity in Your Semiconductor Fabrication**

Chapter 7: New Industry Demands Require New Industry Solutions

1. IHS Markit, **"Executive Summary - Semiconductors in the IoT"**
2) IDC, **"Smartphone Growth Expected to Remain Positive as Shipments Forecast to Grow to 1.7 Billion in 2021, According to IDC"**
3) Market Research Future, **"Autonomous Vehicles Market Size to Observe Steady Growth and Industry Expected to Grow USD 3.6 billion with CAGR 26.2% by 2027"**
4) BI Intelligence, **"FORECAST: IoT Device Installation Base"**
5) Pete Singer, **Semiconductor Manufacturing & Design**
6) **"Historic Paris Agreement on Climate Change"**
7) McKinsey, **"Bringing energy efficiency to the fab"**
8) SPIE Optics.org, **"ASML beats sales target on extra EUV shipment"**
9) Ibid
10) IC Insights, **"Samsung Poised to Become World's Largest Semi Supplier in 2Q17"**
11) IC Insights, **"Pure-Play Foundries Boosting Their Presence in China"**
12) Russ Fischer, **"Intel and Micron and Depreciated Fabs"**
13) **"Reducing Energy and Carbon Footprint at Fabs: A New Focus for SEMI Standards"**
14) McKinsey, **"Bringing energy efficiency to the fab"**
15) Schneider Electric, Ensuring Process Continuity in Your Semiconductor Fabrication

Life Is On | Schneider Electric