"X80 8ch Analog Input IO module" FIRMWARE HISTORY

Modules: BMXAMI0810, BMXAMI0810H, BMXAMI0800

Version #	Date of Publication	Internal reference	Description
SV**1.80**	05/2023	PEP1029926R PEP1018601R	Optimized RAM consistence detection mechanism.

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Version #	Date of Publication	Internal reference	Description
SV**1.70**	08/2021	PEP0646226R	Fixed channel input value frozen when high EMC disturbance injected in specific condition

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Version #	Date of Publication	Internal reference	Description
SV**1.60**	01/2021	PEP0590525R	Optimized the 4 status LEDs (RUN, ERR, I/O, DL) blinking fast mechanism. Under a rare condition , when the inconsistence of data in RAM occurs and could not be recovered autonomously, this issue will be indicated by module healthy bit and 4 status LEDs blinking fast.

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<table>
<tr><th>Version #</th><th>Date of Publication</th><th>Internal reference</th><th>Description</th></tr>
<tr><td rowspan="2">SV1.50</td><td rowspan="2">04/2020</td><td>PEP0555714R</td><td>Optimized acquisition cycle time under quick input signal to be detected.
Below is the acquisition cycle time calculation table and a FAQ FA404316 had been published for this explanation:
<table>
<tr><th colspan="2">BMX AMI 0410/0800/0810</th><th>SV1.0</th><th>SV1.1</th><th>SV1.2</th><th>SV1.3</th><th>SV1.4 (1)</th><th>SV1.5</th></tr>
<tr><td rowspan="2">Acquisition cycle time when below the slew rate threshold (T) (2)</td><td>Normal (Default) (periodic acquisition for all channels)</td><td colspan="6">5 ms (AMI04**)
9 ms (AMI08**)</td></tr>
<tr><td>Fast (periodic acquisition for the declared channels used)</td><td colspan="6">1 ms + 1 ms x number of channels used</td></tr>
<tr><td rowspan="2">Acquisition cycle time when above the slew rate threshold</td><td>AMI0410 (T at normal or fast)</td><td>Value drift (3)</td><td>T x 2 ms</td><td>T x 2 ms</td><td>T x 2 ms</td><td>NA</td><td>16+(Tx2) ms</td></tr>
<tr><td>AMI0800/0810 (T at normal or fast)</td><td>Value frozen (4)</td><td>T x 2 ms</td><td>8+(Tx2) ms</td><td>8+(Tx2) ms</td><td>16+(Tx2) ms</td><td>16+(Tx2) ms</td></tr>
<tr><td colspan="2">Input signal slew rate threshold (unit: mV/ms or mA/ms)</td><td colspan="3">$\frac{23.84\ mV}{T}$ or $\frac{0.09537\ mA}{T}$</td><td colspan="2">$\frac{400\ mV}{T}$ or $\frac{1.6\ mA}{T}$</td></tr>
<tr><td colspan="8">Note:
(1) SV1.4 was only available for BMX AMI 0810RU/HRU
(2) T is the acquisition cycle time when below the slew rate threshold, it might be different between Normal and Fast mode. It will be used in the calculation for acquisition time when above the slew rate threshold and the calculation of threshold.
(3) For SV1.0 the AMI04** channels contain the value drift (till under range or over range) risk, do NOT use.
(4) For SV1.0 the AMI08** channels contain the value frozen risk, do NOT use.</td></tr>
</table>
</td></tr>
<tr><td>PEP0473117R</td><td>Fixed that deviation exceeds specification in user manual (0.15%FS) when any channel sees fast change input (such as 1Hz sine) signal</td></tr>
</table>

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Version #	Date of Publication	Internal reference	Description
SV**1.3**	06/2018	PEP0446999R	Optimized the timing interrupt management coding to eliminate the weakness in the firmware, which could potentially lead to 4 status LEDs (RUN, ERR, I/O, DL) blinking fast.

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Version #	Date of Publication	Internal reference	Description
SV**1.2**	07/2017	PEP0408531R	Fixed that Input Data randomly spikes high on Channel 0 only